Exhibit 8

Exemplar Texas Instruments Accused Products

The following list of Accused Products is exemplary, non-exhaustive, and non-limiting. Greenthread identifies the following specific products to illustrate each category or type of product that constitutes a Texas Instruments Accused Product. Greenthread further asserts claims against all product variations and part numbers of the Texas Instruments Accused Products. All of the below exemplar products were identified by Texas Instruments' website at https://www.ti.com/product-category/new-products.html?releasePeriod=364

	Amplifiers
1.	INA254
2.	OPA2863-QL
3.	INA310B
4.	OPA206
5.	OPA928
	Microcontrollers & Processors
1.	AM69A
2.	TMS320F2800137
3.	AM68A
4.	DRA821U
5.	TDA4VH-Q1
	Digital-to-Analog Converters
1.	DAC53001
2.	DAC63001
3.	DAC53204W
4.	DAC82001
5.	DAC82002
	Analog to Digital Converters
1.	ADS127L21
2.	ADC12DJ5200SE
3.	ADC34RF52
4.	ADS9218
5.	ADS9817
	Digital Clocks

1.	LMK6C
2.	LMK6H
3.	LMK6P
4.	LMK04832-SEP
5.	LMK5B33414
	Interface ICs
1.	DS90UB635-Q1
2.	THVD1454
3.	TCAN1462-Q1
4.	THVD2410V
5.	DS160PR1601
	Audio Processors
1.	TPA3223
2.	TAS2781
3.	PCM5120-Q1
4.	PCM3120-Q1
5.	PCM1820-Q1
	Digital Light Processors
1.	DLP4620S-Q1
2.	DLP4621-Q1
3.	DLP801XE
4.	DLP801RE
5.	DLP301S
	Isolation ICs
1.	ISOW7742-Q1
2.	ISOW7741-Q1
3.	ISOM8710
4.	SN6507-Q1
5.	AMC1400
	Logic & Voltage Translation
1.	SN74LV4T08-Q1

2.	SN74LV165B-EP
3.	SN74LV8T245
4.	SN74LV8T245-Q1
5.	SN74LV164A-Q1
	Motor Drivers
1.	DRV8962
2.	DRV831BC-Q1
3.	DRV8143-Q1
4.	DRV8411A
5.	MCT8329A
	Power Management
1.	LMR36502
2.	TPS65219
3.	LM2105
4.	TPS61033
5.	TPS61299
	Radio Frequency & Microwave ICs
1.	TRF0206-SP
2.	AFE8000
3.	AFE7952
4.	LMX1204
5.	LMX2571-EP
	Sensors
1.	AWR2944
2.	TMAG5170D-Q1
3.	OPT3005
4.	OPT4048
5.	TMP1826
	Switches & Multiplexers
1.	TMUX4053
2.	TMUX4052

3.	TMUX8211
4.	TMUX8213
5.	TMUXHS221
	Wireless Connectivity ICs
1.	CC266R-Q1
2.	CC2651R3SIPA
3.	CC2652PSIP

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

U.S. Patent No. 10,510,842	Accused Products Texas Instruments BQ25123 Battery Charger Power Management IC
[Claim 1, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Texas Instruments Accused Products include a semiconductor device. This chart includes exemplary information regarding a representative example of the Texas Instruments Accused Products, the Texas Instruments BQ25123 Battery Charger Power Management IC ("BQ25123"). The BQ25123 was analyzed in the below-referenced report from Tech Insights. The complete report is hereby incorporated by reference into each and every claim and claim element discussed. "Texas Instruments BQ25123Batter Charger Power Management IC Power Essentials Summary," available at https://library.techinsights.com/search/device-details?tab=reports&id=PEF-2109-802&genealogyCode=TEX-BQ25123YFPT&activeTab=Reports ("BQ25123 Report"). Selected pages are reproduced herein to aid in understanding. Tech Insights techinsights.com Texas Instruments BQ25123 Battery Charger Power Management IC Power Essentials Summary BQ25123 Report at Cover. The Texas Instruments BQ25123 is representative of the Texas Instruments Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other Texas Instruments Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '842 patent (and the other asserted patents). For example, the other Texas Instruments Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '842 patent (and the other asserted patents). The claimed invention would have application in numerous types of Texas Instruments products, including, but not limited to, amplifiers, audio processors, digital-to-analog converters, analog-to-digital converters, digital clocks, interface ICs, isolation ICS, microcontrollers and processors, digital

signal processors, digital light processors, motor drivers, power management, switches & multiplexers, radio frequency and microwave ICs, wireless connectivity ICs, logic & voltage translation, sensors, and other ICs, because such products would benefit from, among other things, improved switching time for transistors in the device. Therefore, upon information and belief the other Texas Instruments Accused Products contain similar features as the Texas Instruments BQ25123 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other Texas Instruments Accused Products contain similar features as the Texas Instruments BQ25123, and function in a similar way with respect to the features claimed in the asserted claims.

This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery. The Texas Instruments Accused Products, of which Texas Instruments BQ25123 is one example, are semiconductor devices.

Device Summary

- This report presents analysis of the Texas Instruments BQ25123 silicon (Si) based power management IC (PMIC). The BQ25123 is a highly-integrated battery charger PMIC geared for wearable applications and rechargeable toys. It features an integrated buck converter with a low I_Q of 700 nA to maximize battery life, supports charge currents from 5 mA to 300 mA, and have I^2C interface programmable parameters [3].
- The BQ25123 is PMIC in a 25-ball wafer level chip scale package (WLCSP), referred to die scale ball grid array (DSBGA) by Texas Instruments [3].
- The BQ25120_A5B die is about 270 µm thick and uses bipolar-CMOS-DMOS (BCD) technology. It features two polysilicon layers for transistor and polysilicon-on-polysilicon (POP) capacitor structures, three aluminum (Al) metal layers with titanium nitride (TiN) barrier layers, tungsten (W) contacts and vias, titanium silicide (TiSi) at the source, drain, and polysilicon contact regions, a phosphosilicate glass (SiOP) pre-metal dielectric (PMD), silicon oxide (SiO) intermetal dielectric (IMD), and SiO and silicon nitride (SiN)* passivation. Local oxidation of silicon (LOCOS) is used for isolation. The redistribution layer (RDL) structure is not analyzed. The die utilizes a P-type substrate with an about 16 µm lighter P-type likely epitaxial layer. The same die is also found in Texas Instruments' BQ25116A.
- Six switching transistor blocks are identified on this device, as shown on page 14. Transistor array Q2 was analyzed and confirmed to be N-channel DMOS with a cell (drain-to-drain) pitch of 5.8 µm and a channel length of about 0.22 µm.
- In the power management (PWM) controller region, the minimum observed gate length is 0.38 µm on a 1.2 µm pitch, and the minimum observed metal pitch is 0.53 µm in metal 1. The results are generally consistent with TechInsights' previous analysis of the Texas Instruments' LBC7 0.25 µm BCD processing technology [4], with a relaxed front end of line (FEOL) geometry.

Manufacturer	Texas Instruments
Part number	BQ25123
Foundry	Texas Instruments
Type	PMIC
Date code	88 (likely 2018 August)
Package type	25-ball WLCSP
Package markings	TI 88C6HRI BQ25123
Package dimensions	2.54 mm × 2.47 mm × 0.47 mm (including bumps)
Die markings	<Texas Instruments logo> (M) TI 2014 BQ25120 A5B
Die size (whole die)	2.54 mm × 2.47 mm
Die size (edge seal)	2.48 mm × 2.41 mm
Minimum measured transistor gate/pitch	0.38 µm/1.2 µm
Minimum measured metal pitch (M1)	0.53 µm
Process generation	0.25 µm
Feature measured to determine process generation	M1 metal pitch, use of TiSi contacts, LOCOS isolation

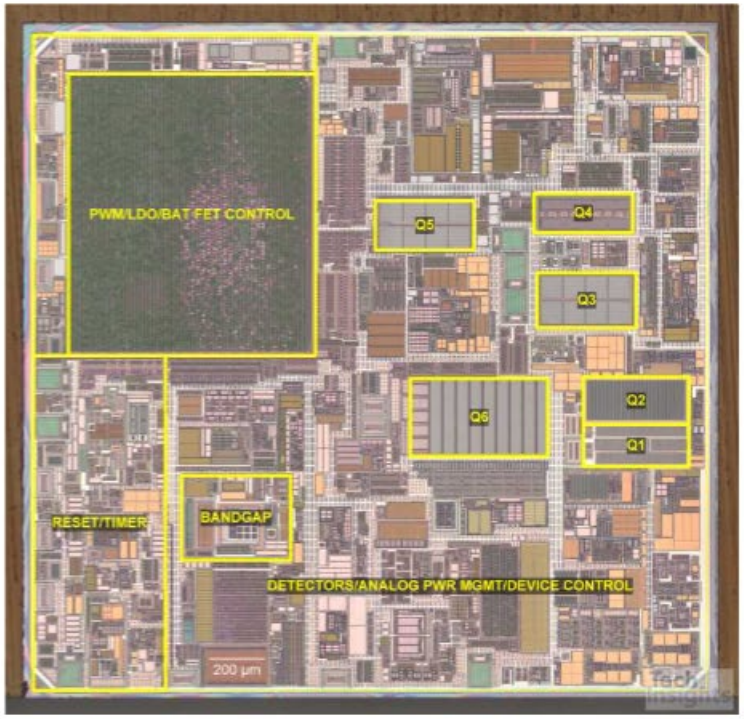
*Note: The top passivation layer is not analyzed and conclusion is based on industry standard structures.

BQ25123 Report at 5.

BQ25120_A5B Die Photograph at the Gate Layer

- The die was deprocessed to the polysilicon gate level.
- The die utilization is characterized in the table below.

Functional Description	Length (mm)	Width (mm)	Area (mm^2)	Percentage of Die
Q1 (switching transistor connected between the DC input supply pin [IN] and the high-side bypass connection pin [PMID])	0.15	0.39	0.06	1.0
Q2 (switching transistor connected between the DC input supply pin [IN] and the high-side bypass connection pin [PMID])	0.17	0.39	0.07	1.1
Q3 (switching transistor connected between the high-side bypass connection pin [PMID] and the inductor connection pin [SW])	0.20	0.36	0.07	1.2
Q4 (switching transistor connected between the inductor connection pin [SW] and the PGND pin [PGND])	0.14	0.36	0.05	0.9
Q5 (switching transistor connected between the input to the load switch pin [VINLS] and the load switch/LDO output pin [LDO])	0.18	0.36	0.06	1.1
Q6 (switching transistor connected between the battery connection pin [BAT] and the high-side bypass connection pin [PMID])	0.28	0.50	0.14	2.4
Bandgap bias generator	0.31	0.40	0.12	2.1
Reset/timer block	1.22	0.48	0.59	9.8
Detectors/analog PWR MGMT/device control block	Irregular		3.50	58.5
PWM control/LDO/BAT FET control	1.03	0.90	0.92	15.5
Control I/O	Irregular		0.28	4.6
Others			0.12	1.8
Total die	2.41	2.48	5.98	100.0



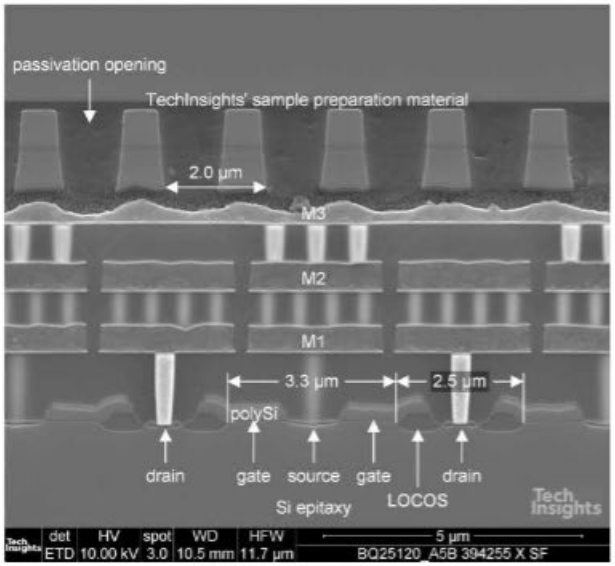
BQ25123YFPT_BQ25120_BPoly_blocks.png

Tech Insights

BQ25123 Report at 14.

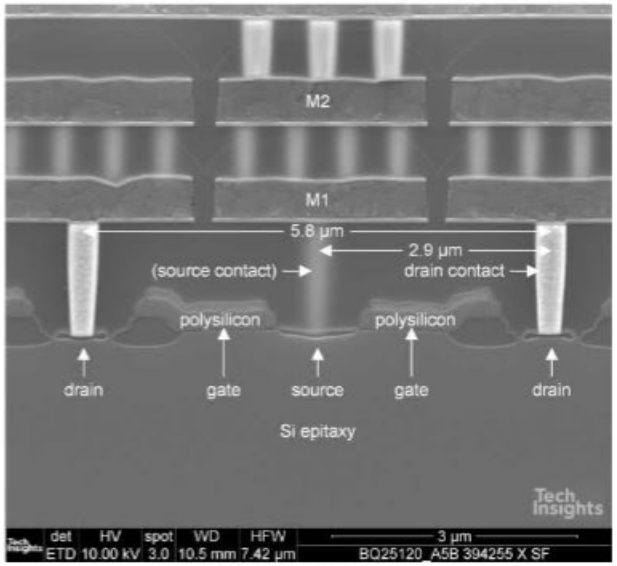
BQ25120_A5B Die Q2 N-LDMOS Array

- The passivation opening pitch for the RDL is 2.0 µm. The RDL is removed in the sample preparation where partial overetch is observed in the metal 3 layer.
- The exposed Si region measures 3.3 µm and the isolation (LOCOS) region, including the central Si for drain contact, measures about 2.5 µm.
- The cell (drain-to-drain) pitch measures about 5.8 µm, and the drain-to-source pitch measures 2.9 µm.



008_HV_block_394254.png

Q2 N-LDMOS Array – SEM Cross Section A-A



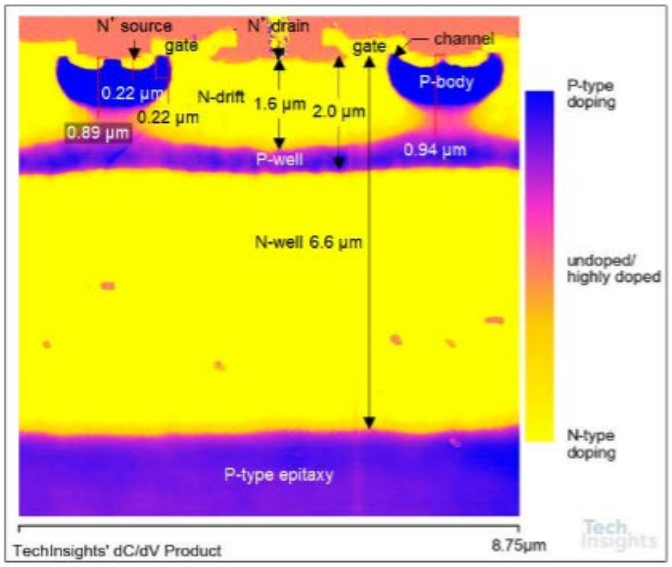
009_HV_block_394254.png

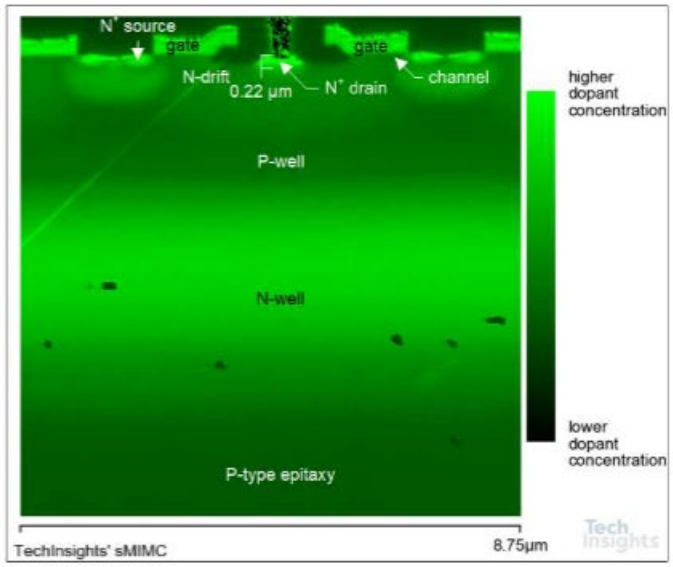
Q2 N-LDMOS Array – SEM Cross Section A-A

BQ25123 Report at 28.

<table>
<tr>
<td></td>
<td>
<h2>BQ25120_A5B Die Q2 N-LDMOS Array – P- and N-Type Regions</h2>

SCM and sMIM-C analysis of the Q2 N-LDMOS show an N-channel device structure with an about 0.22 µm channel length.
The N-well, N-drift, and N+ source/drain (S/D) depths are about 6.6 µm, 1.6 µm, and 0.22 µm, respectively.
The P-body depth is nominally about 0.92 µm and the P-well depth is around 2.0 µm.



array_010722135721_PRODUCT_FRW_8.75u_512p_394254.png
Q2 N-LDMOS – SCM Cross Section A-A


array_010722135721_sMIM-CC_FRW_8.75u_512p_394254.png
Q2 N-LDMOS – sMIM-C Cross Section A-A

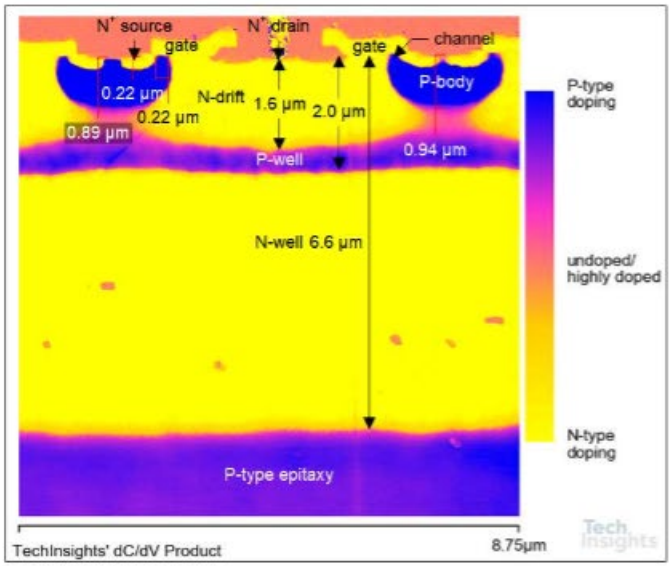
BQ25123 Report at 29.
</td>
</tr>
<tr>
<td>[Claim 1, Element 1] a substrate of a first doping type at a first doping level having first</td>
<td>The Texas Instruments Accused Products include/comprise a semiconductor device comprising a substrate of a first doping type at a first doping level having first and second surfaces. For example, analysis of an exemplary Texas Instruments Accused Product (the Texas Instruments BQ25123 discussed above) reveals the presence of such a substrate.

For example, the Texas Instruments BQ25123 discussed above for Claim 1, Preamble, was imaged using scanning electron microscopy (SEM) scanning capacitance/microwave impedance microscopy (SCM/sMIM) analysis. The SCM image of the LDMOS array shows a P-type substrate epitaxy having a first doping level, the substrate having a first and second surface.</td>
</tr>
</table>

and second surfaces;

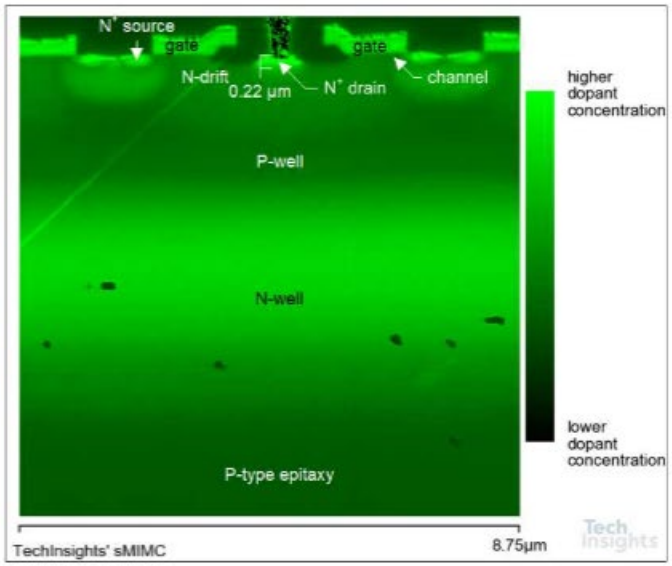
BQ25120_A5B Die Q2 N-LDMOS Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the Q2 N-LDMOS show an N-channel device structure with an about 0.22 µm channel length.
- The N-well, N-drift, and N+ source/drain (S/D) depths are about 6.6 µm, 1.6 µm, and 0.22 µm, respectively.
- The P-body depth is nominally about 0.92 µm and the P-well depth is around 2.0 µm.



array_010722135721_PRODUCT_FRW_8.75u_512p_394254.png

Q2 N-LDMOS – SCM Cross Section A-A

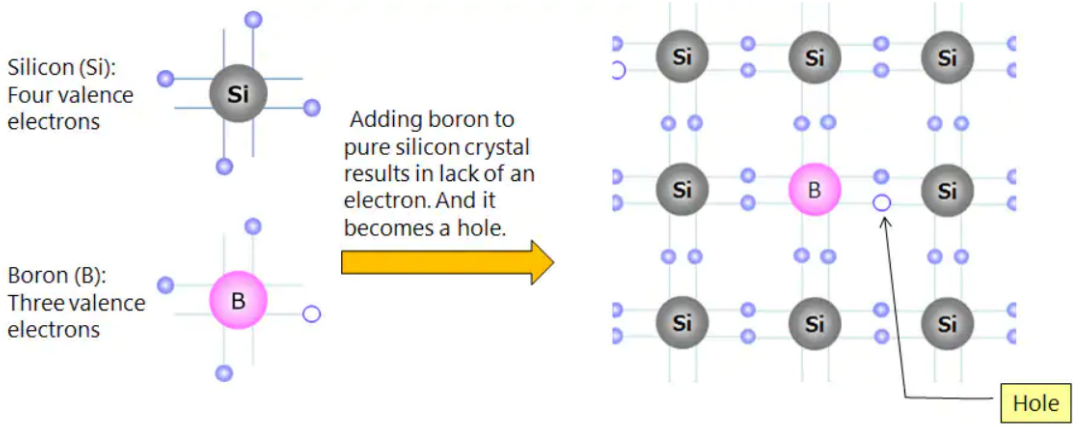


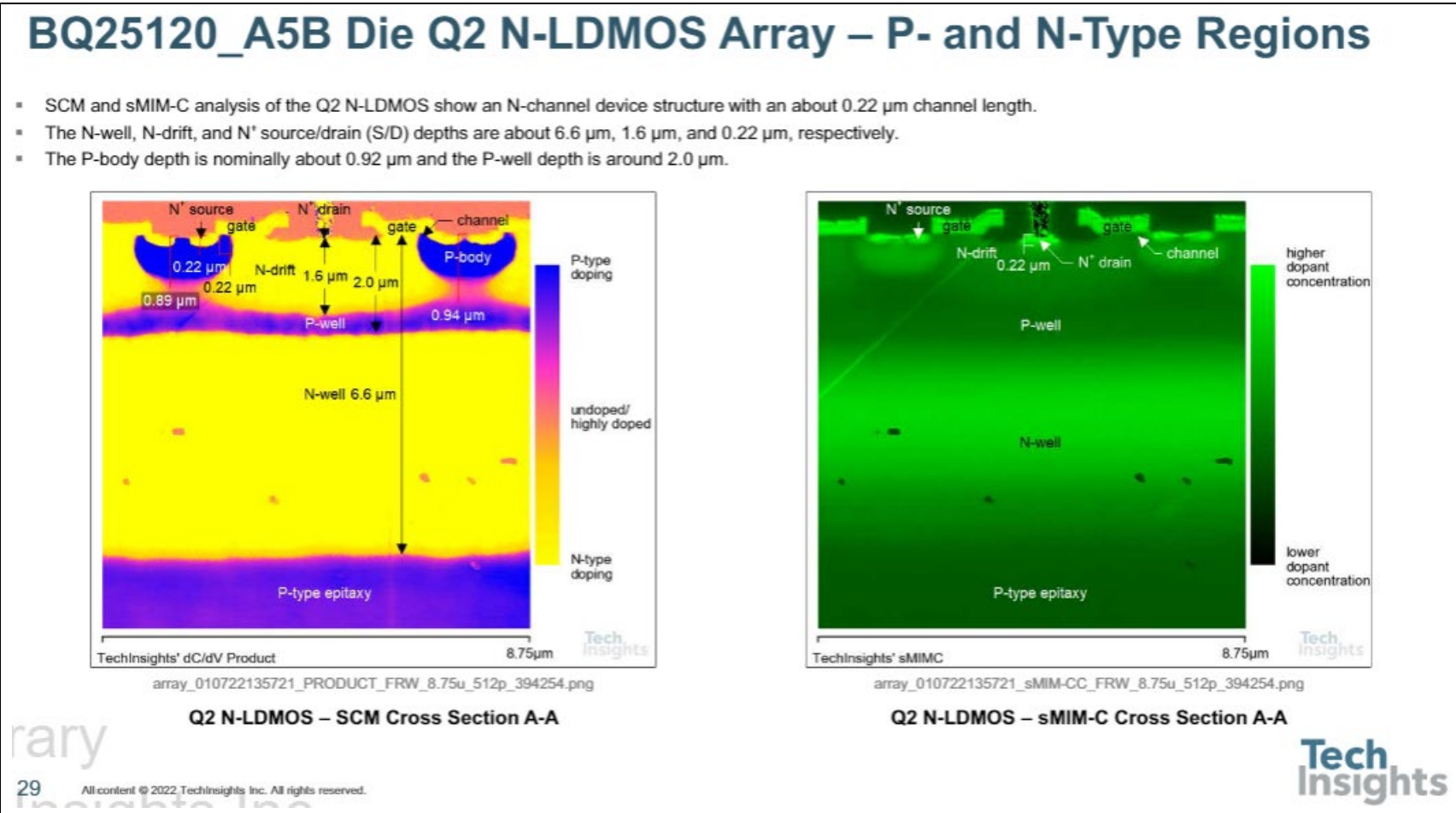
array_010722135721_sMIM-CC_FRW_8.75u_512p_394254.png

Q2 N-LDMOS – sMIM-C Cross Section A-A

29

BQ25123 Report at 29.

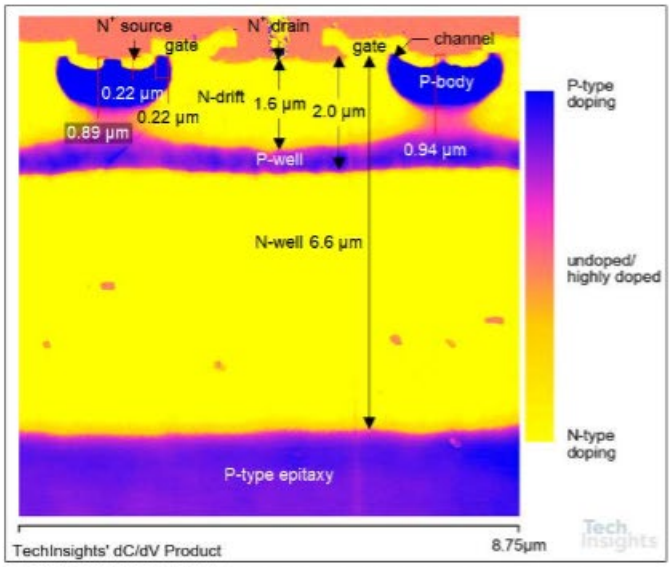
	What is a p-type Semiconductor? A p-type semiconductor is an intrinsic semiconductor doped with boron (B) or indium (In). Silicon of Group IV has four valence electrons and boron of Group III has three valence electrons. If a small amount of boron is doped to a single crystal of silicon, valence electrons will be insufficient at one position to bond silicon and boron, resulting in holes* that lack electrons. When a voltage is applied in this state, the neighboring electrons move to the hole, so that the place where an electron is present becomes a new hole, and the holes appear to move to the "–" electrode in sequence.  * This hole is the carrier of a p-type semiconductor. *See* https://toshiba.semicon-storage.com/us/semiconductor/knowledge/e-learning/discrete/chap1/chap1-4.html#:~:text=A%20p%2Dtype%20semiconductor%20is,III%20has%20three%20valence%20electrons.
[Claim 1, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type	The Texas Instruments Accused Products, and products incorporating them, include/comprise a semiconductor device comprising a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed. For example, as shown in imagery from the Tech Insights Report, the exemplary Texas Instruments BQ25123 scanning capacitance/microwave impedance microscopy (SCM/sMIM) analysis includes a first active region disposed adjacent the first surface of the substrate. See below showing "P- and N-Type Regions," where N-wells and P-wells are formed, the N-wells being disposed adjacent the first surface of the substrate with a second doping type (N-type doping) opposite in conductivity to the first doping type (P-type doping) and within which transistors can be formed. Details regarding formation of transistors are in the possession of Defendants and are expected to be obtained through discovery.

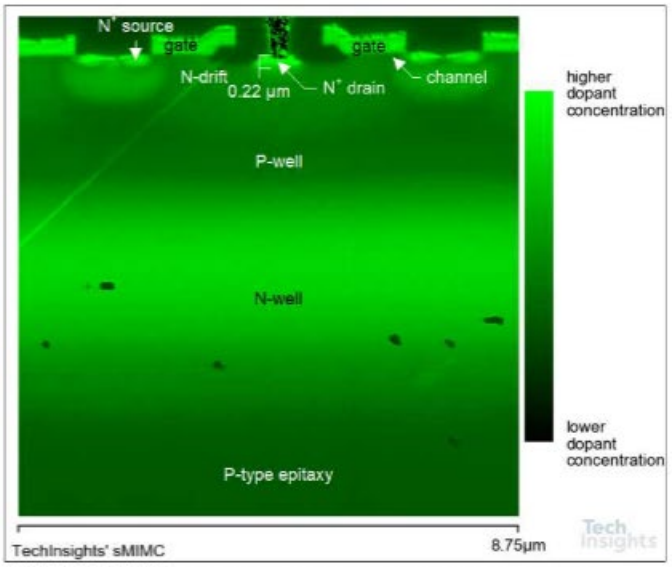
and within which transistors can be formed;	 BQ25123 Report at 29.
[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to	The Texas Instruments Accused Products include a semiconductor device comprising a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed. For example, the gate, drain, and source annotations reproduced at Claim 1, Element 2 show the active region within which transistors can be formed. Details regarding formation of transistors are in the possession of Defendants and are expected to be obtained through discovery.

the first active region and within which transistors can be formed;	
[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region; and	The Texas Instruments Accused Products include a semiconductor device comprising transistors formed in at least one of the first active region or second active region. *See* above at the "P- and N-Type Regions" reproduced at Claim 1, Element 2, shows where N-wells and P-wells are formed, and annotated with source, gate, and drain.
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate.	The Texas Instruments Accused Products meet this limitation. *See* above at Element 1. For example, this is shown by the SIMS and scanning capacitance/microwave impedance microscopy (SCM/sMIM) analysis. SCM/sMIM electrically characterizes the tested device and generates maps which provide graphical representation of the dopant types and concentrations by measuring carrier movement as they are attracted to or repulsed by the probe. The SCM/sMIM maps taken from Texas Instruments Accused Products shown herein demonstrate differences in carrier concentration as a function of depth, which generate electric fields within the accused products. The contrast in the SMIM image is proportional to the capacitance of the sample under inspection, so that brighter green corresponds to higher dopant concentration, and darker green/black corresponds to lower dopant concentration. Likewise, the SCM images above show doping concentration and doping type as indicated in the legends to the right.

<table>
<tr>
<td></td>
<td>
<h2>BQ25120_A5B Die Q2 N-LDMOS Array – P- and N-Type Regions</h2>

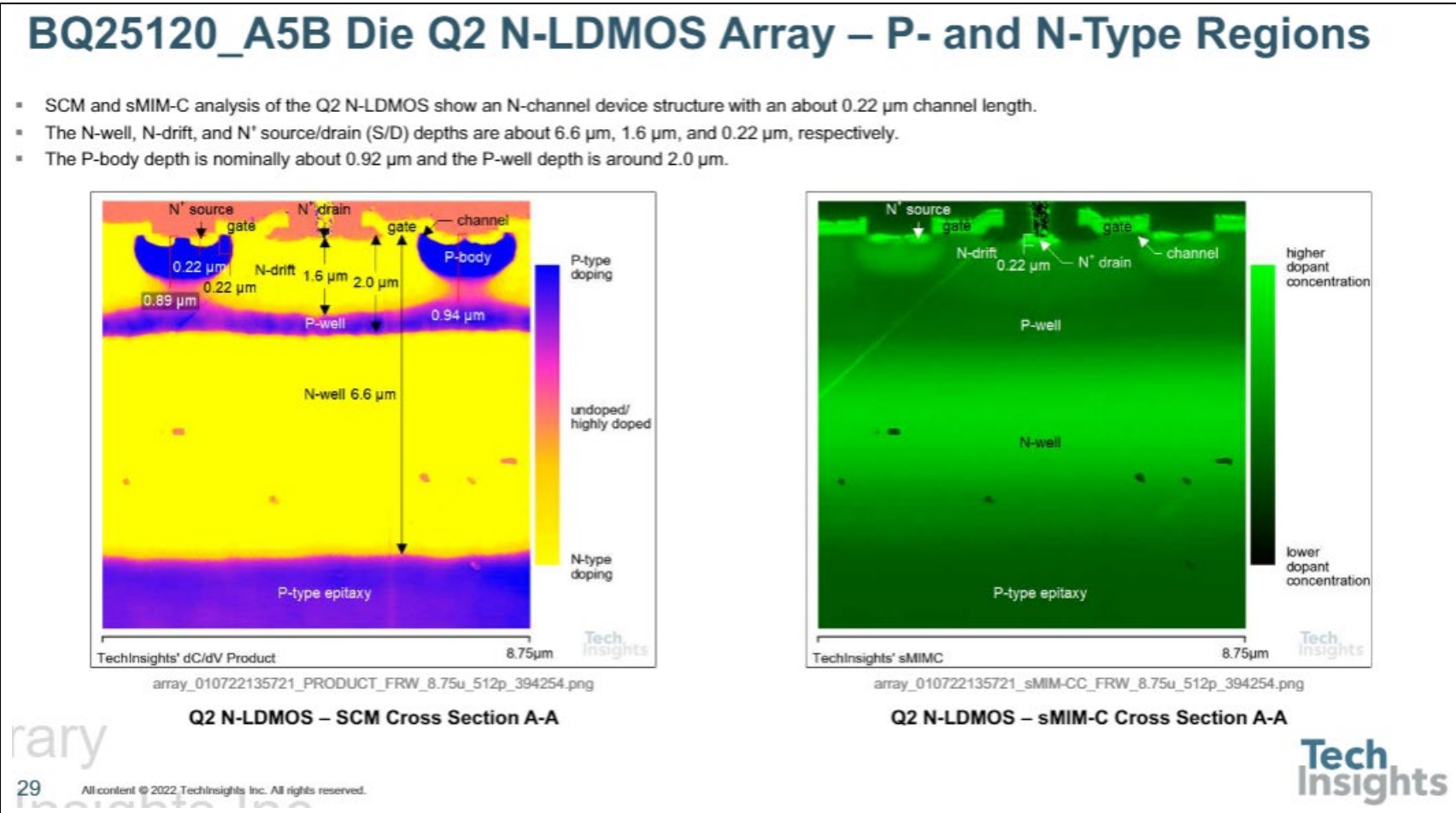
SCM and sMIM-C analysis of the Q2 N-LDMOS show an N-channel device structure with an about 0.22 µm channel length.
The N-well, N-drift, and N+ source/drain (S/D) depths are about 6.6 µm, 1.6 µm, and 0.22 µm, respectively.
The P-body depth is nominally about 0.92 µm and the P-well depth is around 2.0 µm.

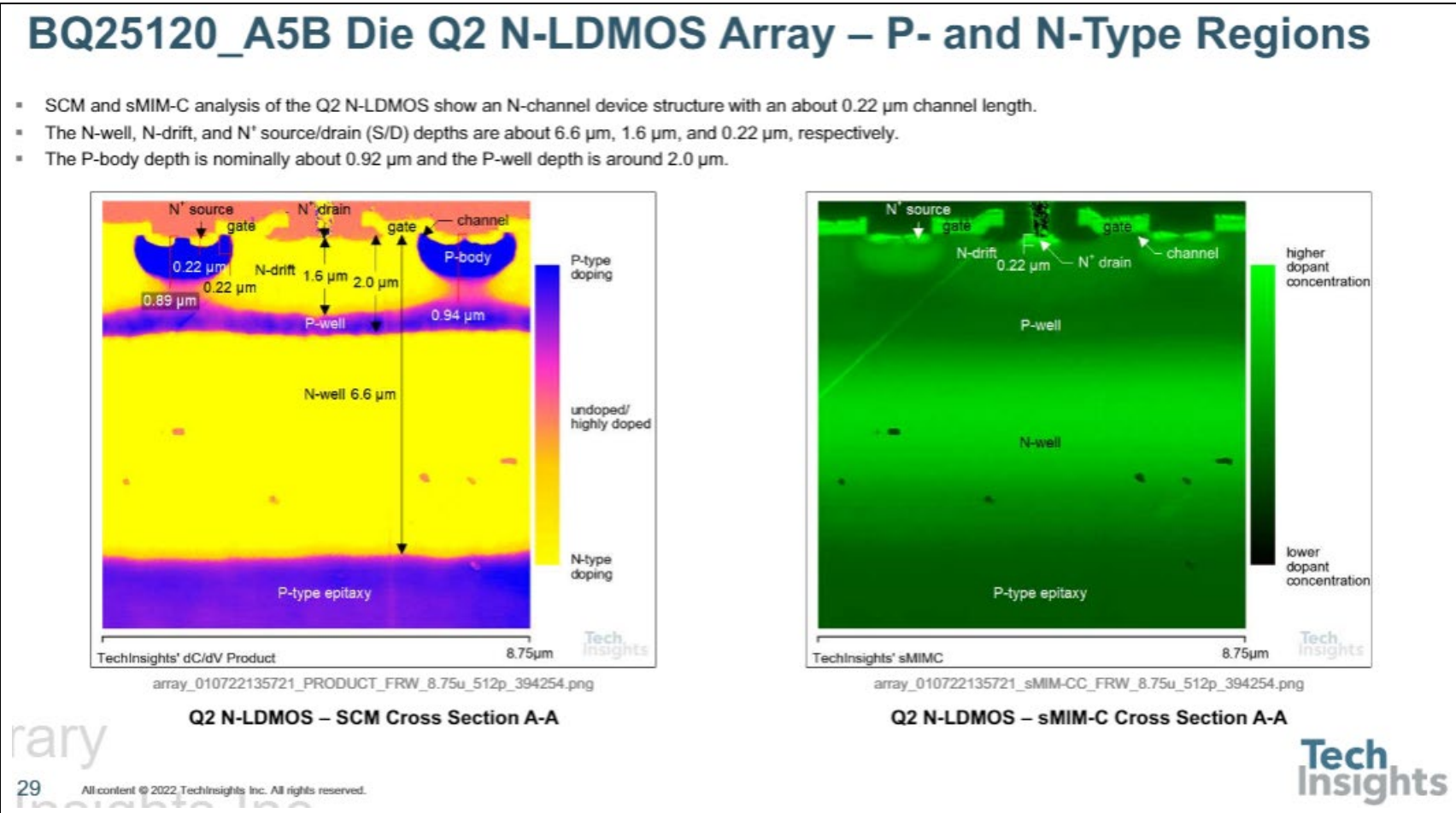


array_010722135721_PRODUCT_FRW_8.75u_512p_394254.png
Q2 N-LDMOS – SCM Cross Section A-A


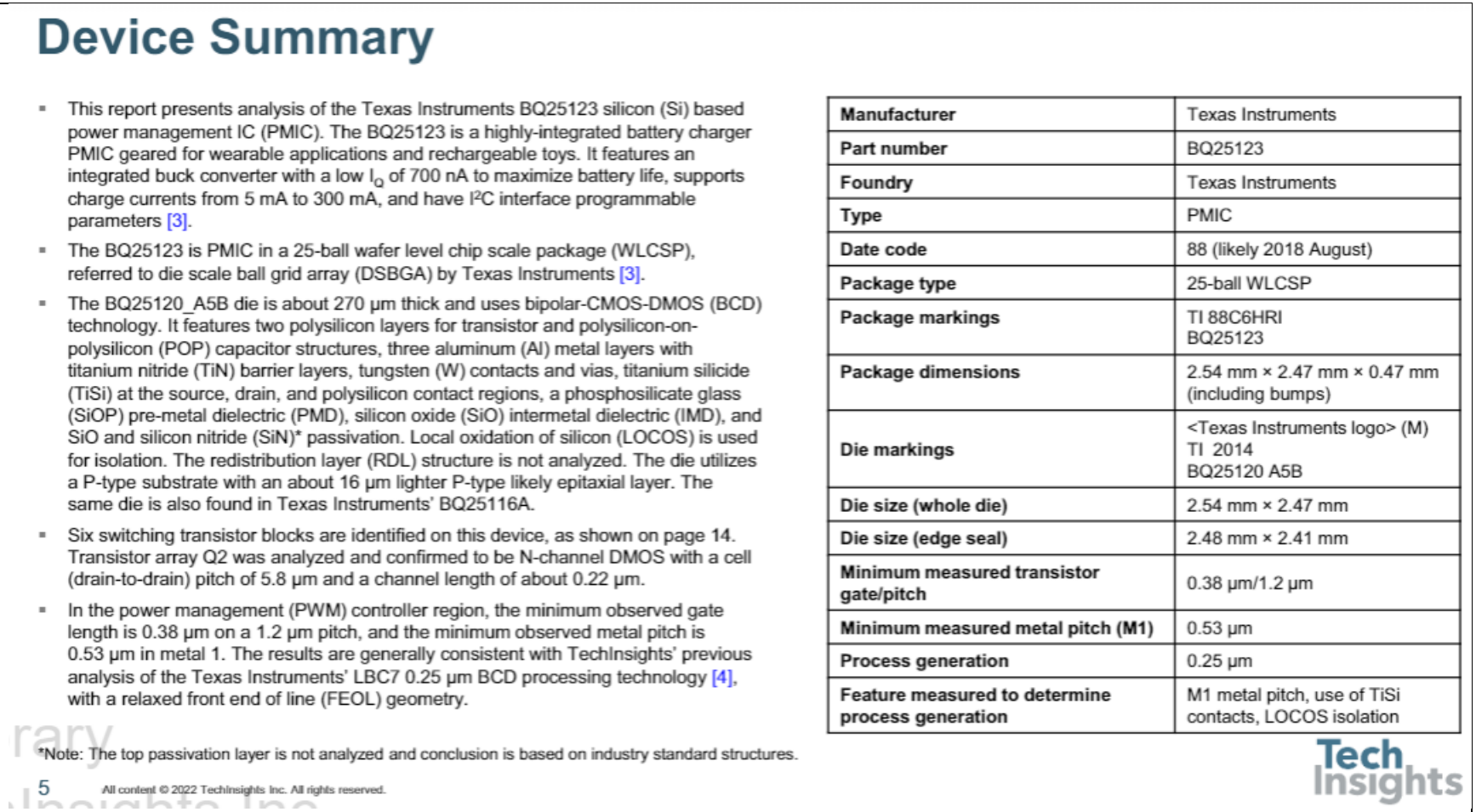
array_010722135721_sMIM-CC_FRW_8.75u_512p_394254.png
Q2 N-LDMOS – sMIM-C Cross Section A-A

BQ25123 Report at 29.</td>
</tr>
<tr>
<td>2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate.</td>
<td>Upon information and belief, the substrate of the Texas Instruments Accused Products has epitaxial silicon on top of a nonepitaxial substrate.
The SCM cross-section image below identifies a P-type epitaxy.</td>
</tr>
</table>

	 BQ25123 Report at 29.
4. The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a	Upon information and belief, the substrate of the Texas Instruments Accused Products has epitaxial silicon on top of a nonepitaxial substrate. The SCM cross-section image below identifies a P-type epitaxy.

nonepitaxial substrate.	 BQ25123 Report at 29.
5. The semiconductor device of claim 1, wherein the first active region and second active region contain	The Texas Instruments Accused Products meet this limitation. As shown above, both N-well and P-wells are used in this device. The first and second active regions accordingly contain p-channel or n-channel devices. *See* Tech Insights Report images reproduced at Claim 1, Element 2.

one of either p-channel and n-channel devices.	
6. The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.	The Texas Instruments Accused Products meet this limitation. As shown above, both N-well and P-wells are used in this device, and the wells include graded dopants. The first and second active regions accordingly contain p-channel or n-channel devices. *See* Tech Insights Report images reproduced at Claim 1, Element 2.
7. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	Upon information and belief, the substrate of the Texas Instruments Accused Products have isolation regions that separate the first and second active regions. As shown in the Device Summary below, "[l]ocal oxidation of silicon (LOCOS) is used for isolation."



Device Summary

- This report presents analysis of the Texas Instruments BQ25123 silicon (Si) based power management IC (PMIC). The BQ25123 is a highly-integrated battery charger PMIC geared for wearable applications and rechargeable toys. It features an integrated buck converter with a low I_Q of 700 nA to maximize battery life, supports charge currents from 5 mA to 300 mA, and have I^2C interface programmable parameters [3].
- The BQ25123 is PMIC in a 25-ball wafer level chip scale package (WLCSP), referred to die scale ball grid array (DSBGA) by Texas Instruments [3].
- The BQ25120_A5B die is about 270 µm thick and uses bipolar-CMOS-DMOS (BCD) technology. It features two polysilicon layers for transistor and polysilicon-on-polysilicon (POP) capacitor structures, three aluminum (Al) metal layers with titanium nitride (TiN) barrier layers, tungsten (W) contacts and vias, titanium silicide (TiSi) at the source, drain, and polysilicon contact regions, a phosphosilicate glass (SiOP) pre-metal dielectric (PMD), silicon oxide (SiO) intermetal dielectric (IMD), and SiO and silicon nitride (SiN)* passivation. Local oxidation of silicon (LOCOS) is used for isolation. The redistribution layer (RDL) structure is not analyzed. The die utilizes a P-type substrate with an about 16 µm lighter P-type likely epitaxial layer. The same die is also found in Texas Instruments' BQ25116A.
- Six switching transistor blocks are identified on this device, as shown on page 14. Transistor array Q2 was analyzed and confirmed to be N-channel DMOS with a cell (drain-to-drain) pitch of 5.8 µm and a channel length of about 0.22 µm.
- In the power management (PWM) controller region, the minimum observed gate length is 0.38 µm on a 1.2 µm pitch, and the minimum observed metal pitch is 0.53 µm in metal 1. The results are generally consistent with TechInsights' previous analysis of the Texas Instruments' LBC7 0.25 µm BCD processing technology [4], with a relaxed front end of line (FEOL) geometry.

Manufacturer	Texas Instruments
Part number	BQ25123
Foundry	Texas Instruments
Type	PMIC
Date code	88 (likely 2018 August)
Package type	25-ball WLCSP
Package markings	TI 88C6HRI BQ25123
Package dimensions	2.54 mm × 2.47 mm × 0.47 mm (including bumps)
Die markings	<Texas Instruments logo> (M) TI 2014 BQ25120 A5B
Die size (whole die)	2.54 mm × 2.47 mm
Die size (edge seal)	2.48 mm × 2.41 mm
Minimum measured transistor gate/pitch	0.38 µm/1.2 µm
Minimum measured metal pitch (M1)	0.53 µm
Process generation	0.25 µm
Feature measured to determine process generation	M1 metal pitch, use of TiSi contacts, LOCOS isolation

*Note: The top passivation layer is not analyzed and conclusion is based on industry standard structures.

BQ25123 Report at 5.

8. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion	Upon information and belief, the graded dopant is fabricated with an ion implantation process. For example, ion implantation is the prevalent process for implementing doping in semiconductor devices, and is believed to be used for the Texas Instruments Accused Products. Additionally Texas Instruments has multiple patents disclosing ion implantation used in semiconductor fabrication, including U.S. Patent No. 9,064,903 which states that "MOS transistors are generally constructed by way of a counter-doping ion implantation into the channel region...." Because Texas Instruments has patents disclosing this practice, and because it is well known in the art, Texas Instruments Accused Products likely meet this limitation. Information about the fabrication process for the Texas Instruments Accused Products, including usage of an ion implantation process, is in the possession of Defendant and is expected to be obtained through discovery.

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

implantation process.	
[Claim 9, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Texas Instruments Accused Products include a semiconductor device. *See* above at Claim 1, Preamble.
[Claim 9, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The Texas Instruments Accused Products meet this limitation. *See* above at Claim 1, Element 1.
[Claim 9, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The Texas Instruments Accused Products meet this limitation. *See* above at Claim 1, Element 2.
[Claim 9, Element 3] a	The Texas Instruments Accused Products meet this limitation. *See* above at Claim 1, Element 3.

second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	
[Claim 9, Element 4] transistors formed in at least one of the first active region or second active region; and	The Texas Instruments Accused Products meet this limitation. *See* above at Claim 1, Element 4.
[Claim 9, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate.	The Texas Instruments Accused Products meet this limitation. *See* above at Claim 1, Element 5.

10. The semiconductor device of claim 9, wherein the substrate is a p-type substrate.	The Texas Instruments Accused Products meet this limitation. *See* above at Claim 2.
12. The semiconductor device of claim 9, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The Texas Instruments Accused Products meet this limitation. *See* above at Claim 4.
13. The semiconductor device of claim 9, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	The Texas Instruments Accused Products meet this limitation. *See* above at Claim 5.
14. The semiconductor device of claim 9, wherein the first active region and	The Texas Instruments Accused Products meet this limitation. *See* above at Claim 6.

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.	
15. The semiconductor device of claim 9, wherein the first active region and second active region are each separated by at least one isolation region.	Upon information and belief, the Texas Instruments Accused Products meet this limitation. *See* above at Claim 7.
16. The semiconductor device of claim 9, wherein the graded dopant is fabricated with an ion implantation process.	Upon information and belief, the Texas Instruments Accused Products meet this limitation. *See* above at Claim 8.
17. The semiconductor device of claim 1, wherein the	The Texas Instruments Accused Products meet this limitation. *See* above at Claim 1, Elements 2-3.

first and second active regions are formed adjacent the first surface of the substrate.	
18. The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring a source, a drain, a gate and a channel region.	The Texas Instruments Accused Products meet this limitation. As discussed above for Claim 1, the Texas Instruments Accused Products include first and second active regions. Upon information and belief, CMOS transistors formed in the first and second active regions, the CMOS transistors requiring a source, a drain, a gate, and a channel region. Details regarding transistors used are in the possession of Defendants and are expected to be obtained through discovery.

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

U.S. Patent No. 10,734,481	Exemplary Accused Product Texas Instruments BQ25123 Battery Charger Power Management IC
[Claim 1, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Texas Instruments Accused Products include a semiconductor device. This chart includes exemplary information regarding a representative example of the Texas Instruments Accused Products, the Texas Instruments BQ25123 Battery Charger Power Management IC ("BQ25123"). The BQ25123 was analyzed in the below-referenced report from Tech Insights. The complete report is hereby incorporated by reference into each and every claim and claim element discussed. "Texas Instruments BQ25123Batter Charger Power Management IC Power Essentials Summary," available at https://library.techinsights.com/search/device-details?tab=reports&id=PEF-2109-802&genealogyCode=TEX-BQ25123YFPT&activeTab=Reports ("BQ25123 Report"). Selected pages are reproduced herein to aid in understanding. Tech Insights techinsights.com Texas Instruments BQ25123 Battery Charger Power Management IC Power Essentials Summary BQ25123 Report at Cover. The Texas Instruments BQ25123 is representative of the Texas Instruments Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other Texas Instruments Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '481 patent (and the other asserted patents). For example, the other Texas Instruments Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '481 patent (and the other asserted patents). The claimed invention would have application in numerous types of Texas Instruments products, including, but not limited to, amplifiers, audio processors, digital-to-analog converters, analog-to-digital converters, digital clocks, interface ICs, isolation ICS, microcontrollers and

processors, digital signal processors, digital light processors, motor drivers, power management, switches & multiplexers, radio frequency and microwave ICs, wireless connectivity ICs, logic & voltage translation, sensors, and other ICs, because such products would benefit from, among other things, improved switching time for transistors in the device. Therefore, upon information and belief the other Texas Instruments Accused Products contain similar features as the Texas Instruments BQ25123 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other Texas Instruments Accused Products contain similar features as the Texas Instruments BQ25123, and function in a similar way with respect to the features claimed in the asserted claims.

This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery. The Texas Instruments Accused Products, of which Texas Instruments BQ25123 is one example, are semiconductor devices.

Device Summary

- This report presents analysis of the Texas Instruments BQ25123 silicon (Si) based power management IC (PMIC). The BQ25123 is a highly-integrated battery charger PMIC geared for wearable applications and rechargeable toys. It features an integrated buck converter with a low I_Q of 700 nA to maximize battery life, supports charge currents from 5 mA to 300 mA, and have I^2C interface programmable parameters [3].
- The BQ25123 is PMIC in a 25-ball wafer level chip scale package (WLCSP), referred to die scale ball grid array (DSBGA) by Texas Instruments [3].
- The BQ25120_A5B die is about 270 µm thick and uses bipolar-CMOS-DMOS (BCD) technology. It features two polysilicon layers for transistor and polysilicon-on-polysilicon (POP) capacitor structures, three aluminum (Al) metal layers with titanium nitride (TiN) barrier layers, tungsten (W) contacts and vias, titanium silicide (TiSi) at the source, drain, and polysilicon contact regions, a phosphosilicate glass (SiOP) pre-metal dielectric (PMD), silicon oxide (SiO) intermetal dielectric (IMD), and SiO and silicon nitride (SiN)* passivation. Local oxidation of silicon (LOCOS) is used for isolation. The redistribution layer (RDL) structure is not analyzed. The die utilizes a P-type substrate with an about 16 µm lighter P-type likely epitaxial layer. The same die is also found in Texas Instruments' BQ25116A.
- Six switching transistor blocks are identified on this device, as shown on page 14. Transistor array Q2 was analyzed and confirmed to be N-channel DMOS with a cell (drain-to-drain) pitch of 5.8 µm and a channel length of about 0.22 µm.
- In the power management (PWM) controller region, the minimum observed gate length is 0.38 µm on a 1.2 µm pitch, and the minimum observed metal pitch is 0.53 µm in metal 1. The results are generally consistent with TechInsights' previous analysis of the Texas Instruments' LBC7 0.25 µm BCD processing technology [4], with a relaxed front end of line (FEOL) geometry.

Manufacturer	Texas Instruments
Part number	BQ25123
Foundry	Texas Instruments
Type	PMIC
Date code	88 (likely 2018 August)
Package type	25-ball WLCSP
Package markings	TI 88C6HRI BQ25123
Package dimensions	2.54 mm × 2.47 mm × 0.47 mm (including bumps)
Die markings	<Texas Instruments logo> (M) TI 2014 BQ25120 A5B
Die size (whole die)	2.54 mm × 2.47 mm
Die size (edge seal)	2.48 mm × 2.41 mm
Minimum measured transistor gate/pitch	0.38 µm/1.2 µm
Minimum measured metal pitch (M1)	0.53 µm
Process generation	0.25 µm
Feature measured to determine process generation	M1 metal pitch, use of TiSi contacts, LOCOS isolation

*Note: The top passivation layer is not analyzed and conclusion is based on industry standard structures.

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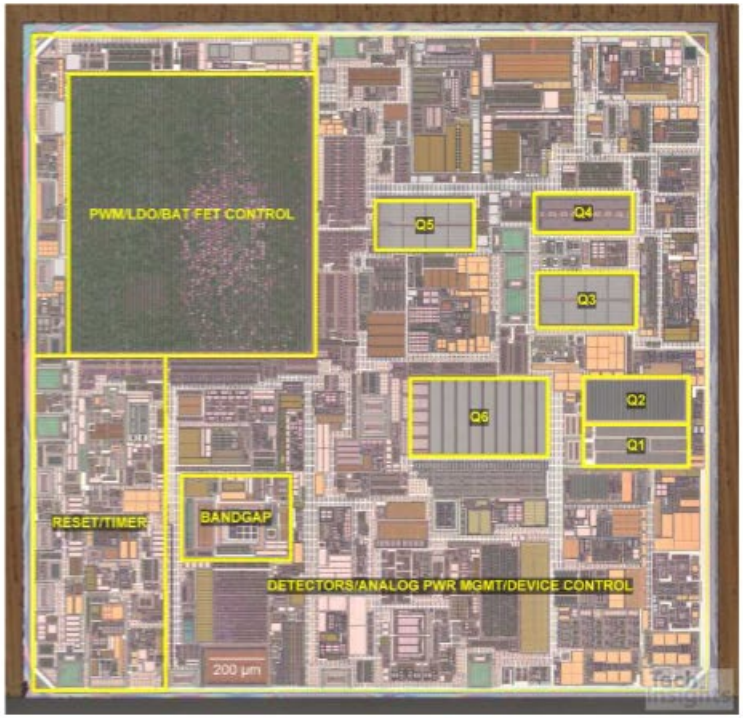
Tech Insights

BQ25123 Report at 5.

BQ25120_A5B Die Photograph at the Gate Layer

- The die was deprocessed to the polysilicon gate level.
- The die utilization is characterized in the table below.

Functional Description	Length (mm)	Width (mm)	Area (mm^2)	Percentage of Die
Q1 (switching transistor connected between the DC input supply pin [IN] and the high-side bypass connection pin [PMID])	0.15	0.39	0.06	1.0
Q2 (switching transistor connected between the DC input supply pin [IN] and the high-side bypass connection pin [PMID])	0.17	0.39	0.07	1.1
Q3 (switching transistor connected between the high-side bypass connection pin [PMID] and the inductor connection pin [SW])	0.20	0.36	0.07	1.2
Q4 (switching transistor connected between the inductor connection pin [SW] and the PGND pin [PGND])	0.14	0.36	0.05	0.9
Q5 (switching transistor connected between the input to the load switch pin [VINLS] and the load switch/LDO output pin [LDO])	0.18	0.36	0.06	1.1
Q6 (switching transistor connected between the battery connection pin [BAT] and the high-side bypass connection pin [PMID])	0.28	0.50	0.14	2.4
Bandgap bias generator	0.31	0.40	0.12	2.1
Reset/timer block	1.22	0.48	0.59	9.8
Detectors/analog PWR MGMT/device control block	Irregular		3.50	58.5
PWM control/LDO/BAT FET control	1.03	0.90	0.92	15.5
Control I/O	Irregular		0.28	4.6
Others			0.12	1.8
Total die	2.41	2.48	5.98	100.0



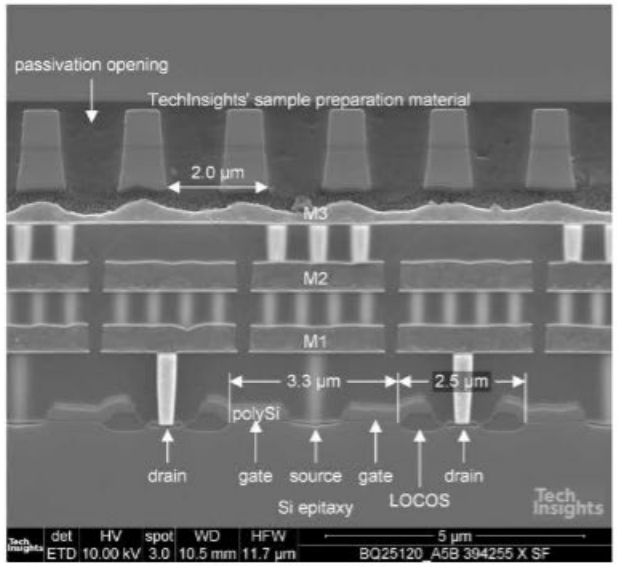
BQ25123YFPT_BQ25120_BPoly_blocks.png

Tech Insights

BQ25123 Report at 14.

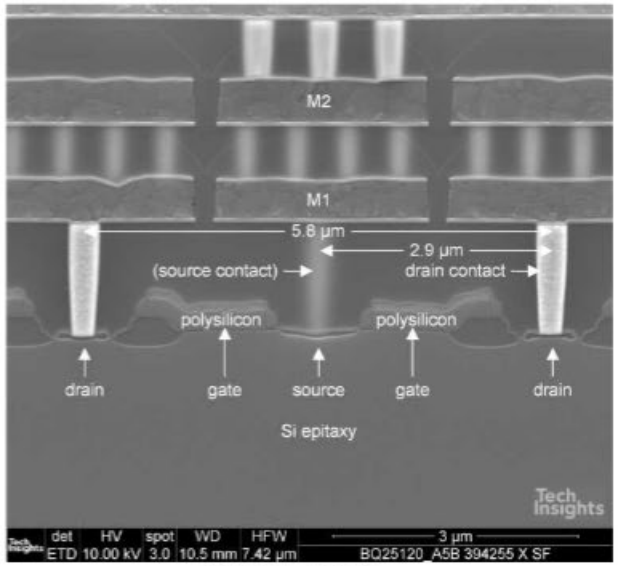
BQ25120_A5B Die Q2 N-LDMOS Array

- The passivation opening pitch for the RDL is 2.0 µm. The RDL is removed in the sample preparation where partial overetch is observed in the metal 3 layer.
- The exposed Si region measures 3.3 µm and the isolation (LOCOS) region, including the central Si for drain contact, measures about 2.5 µm.
- The cell (drain-to-drain) pitch measures about 5.8 µm, and the drain-to-source pitch measures 2.9 µm.



008_HV_block_394254.png

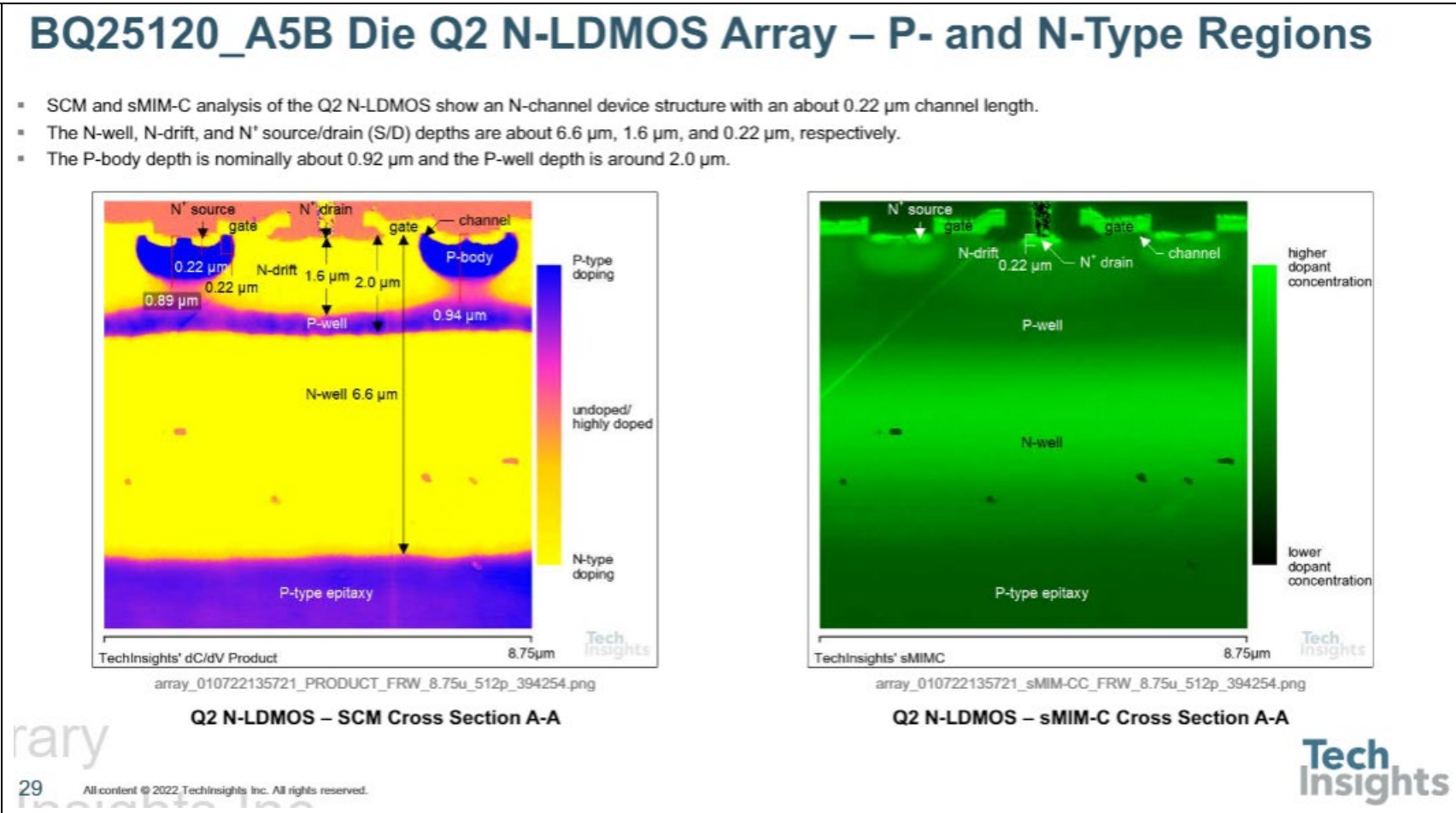
Q2 N-LDMOS Array – SEM Cross Section A-A



009_HV_block_394254.png

Q2 N-LDMOS Array – SEM Cross Section A-A

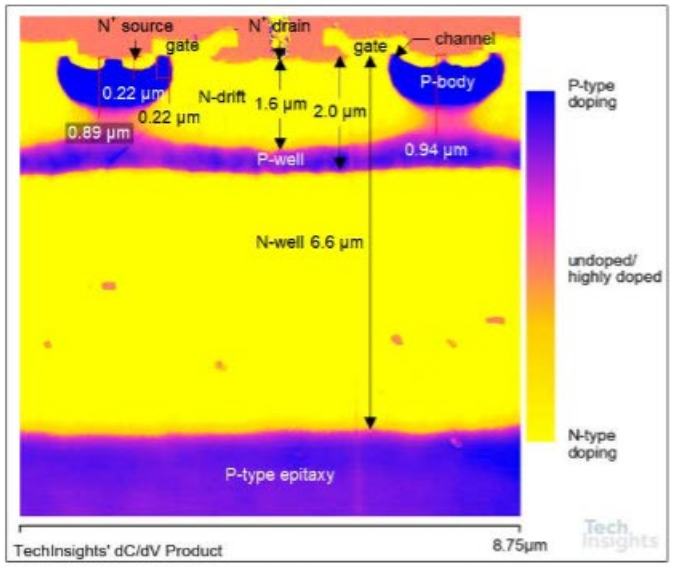
BQ25123 Report at 28.

	 BQ25123 Report at 29.
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having first	The Texas Instruments Accused Products include/comprise a semiconductor device comprising a substrate of a first doping type at a first doping level having first and second surfaces. For example, analysis of an exemplary Texas Instruments Accused Product (the Texas Instruments BQ25123 discussed above) reveals the presence of such a substrate. For example, the Texas Instruments BQ25123 discussed above for Claim 1, Preamble, was imaged using scanning electron microscopy (SEM) scanning capacitance/microwave impedance microscopy (SCM/sMIM) analysis. The SCM image of the LDMOS array shows a P-type substrate epitaxy having a first doping level, the substrate having a first and second surface.

and second surfaces;

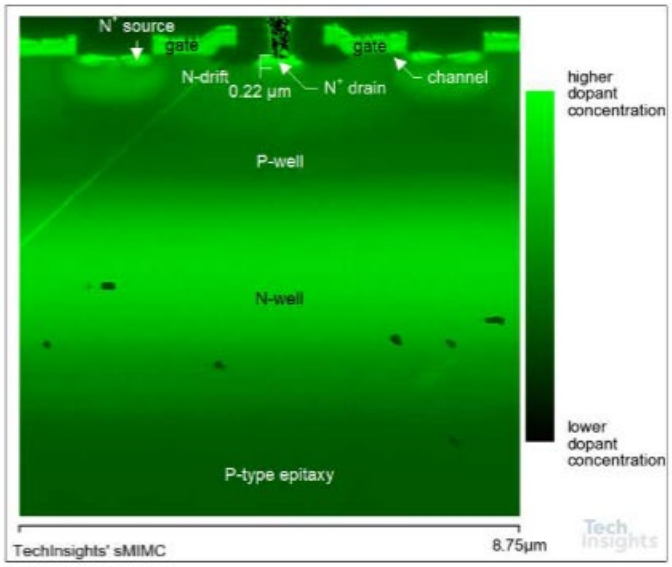
BQ25120_A5B Die Q2 N-LDMOS Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the Q2 N-LDMOS show an N-channel device structure with an about 0.22 µm channel length.
- The N-well, N-drift, and N+ source/drain (S/D) depths are about 6.6 µm, 1.6 µm, and 0.22 µm, respectively.
- The P-body depth is nominally about 0.92 µm and the P-well depth is around 2.0 µm.



array_010722135721_PRODUCT_FRW_8.75u_512p_394254.png

Q2 N-LDMOS – SCM Cross Section A-A



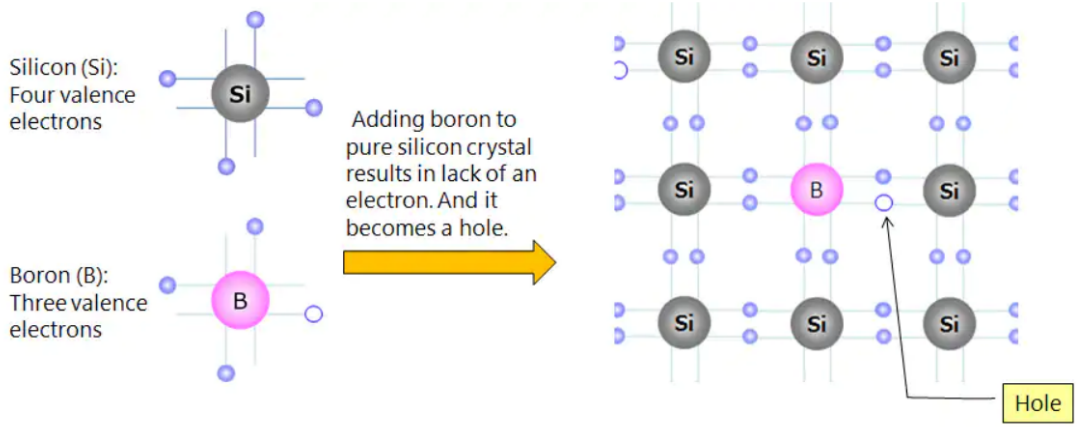
array_010722135721_sMIM-CC_FRW_8.75u_512p_394254.png

Q2 N-LDMOS – sMIM-C Cross Section A-A

29

BQ25123 Report at 29.

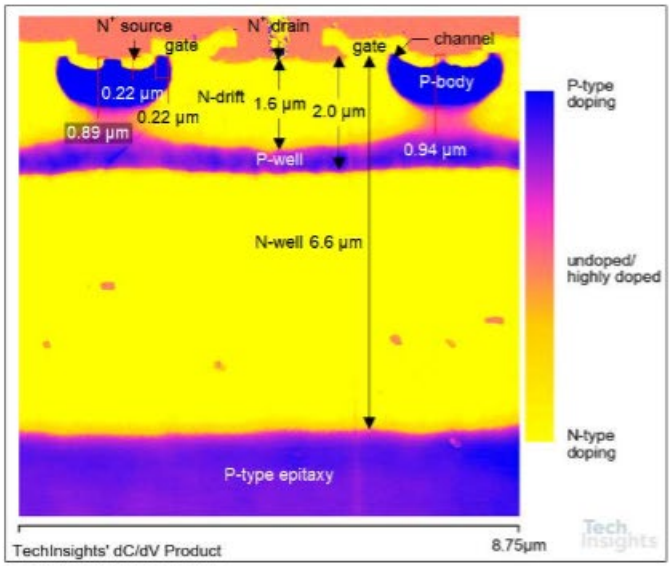
Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

	What is a p-type Semiconductor? A p-type semiconductor is an intrinsic semiconductor doped with boron (B) or indium (In). Silicon of Group IV has four valence electrons and boron of Group III has three valence electrons. If a small amount of boron is doped to a single crystal of silicon, valence electrons will be insufficient at one position to bond silicon and boron, resulting in holes* that lack electrons. When a voltage is applied in this state, the neighboring electrons move to the hole, so that the place where an electron is present becomes a new hole, and the holes appear to move to the "–" electrode in sequence.  * This hole is the carrier of a p-type semiconductor. *See* https://toshiba.semicon-storage.com/us/semiconductor/knowledge/e-learning/discrete/chap1/chap1-4.html#:~:text=A%20p%2Dtype%20semiconductor%20is,III%20has%20three%20valence%20electrons.
[Claim 1, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which	The Texas Instruments Accused Products, and products incorporating them, include/comprise a semiconductor device comprising a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed. For example, as shown in imagery from the Tech Insights Report, the exemplary Texas Instruments BQ25123 scanning capacitance/microwave impedance microscopy (SCM/sMIM) analysis includes a first active region disposed adjacent the first surface of the substrate. See below showing "P- and N-Type Regions," where N-wells and P-wells are formed, the N-wells being disposed adjacent the first surface of the substrate with a second doping type (N-type doping) opposite in conductivity to the first doping type (P-type doping) and within which transistors can be formed. Details regarding formation of transistors are in the possession of Defendants and are expected to be obtained through discovery.

transistors can be formed;

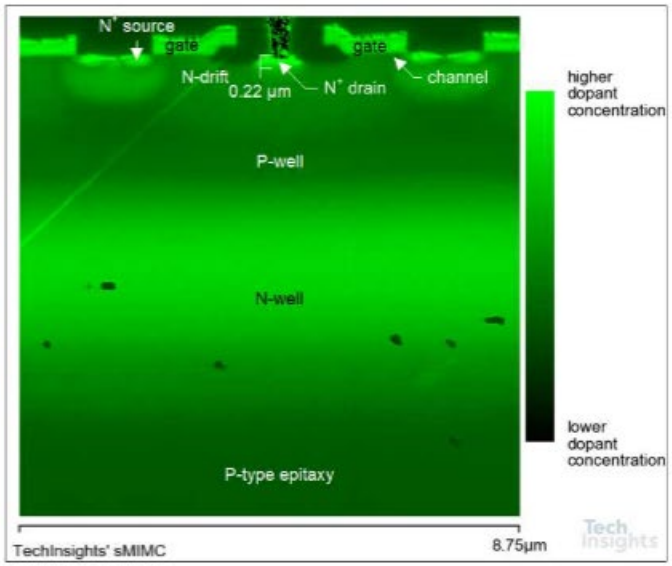
BQ25120_A5B Die Q2 N-LDMOS Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the Q2 N-LDMOS show an N-channel device structure with an about 0.22 µm channel length.
- The N-well, N-drift, and N+ source/drain (S/D) depths are about 6.6 µm, 1.6 µm, and 0.22 µm, respectively.
- The P-body depth is nominally about 0.92 µm and the P-well depth is around 2.0 µm.



array_010722135721_PRODUCT_FRW_8.75u_512p_394254.png

Q2 N-LDMOS – SCM Cross Section A-A



array_010722135721_sMIM-CC_FRW_8.75u_512p_394254.png

Q2 N-LDMOS – sMIM-C Cross Section A-A

BQ25123 Report at 29.

[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active	The Texas Instruments Accused Products include a semiconductor device comprising a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed. For example, the gate, drain, and source annotations reproduced at Claim 1, Element 2 show the active region within which transistors can be formed. Details regarding formation of transistors are in the possession of Defendants and are expected to be obtained through discovery.

region and within which transistors can be formed;	
[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region;	The Texas Instruments Accused Products include a semiconductor device comprising transistors formed in at least one of the first active region or second active region. *See* above at the "P- and N-Type Regions" reproduced at Claim 1, Element 2, shows where N-wells and P-wells are formed, and annotated with source, gate, and drain.
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate; and	The Texas Instruments Accused Products meet this limitation. *See* above at Element 1. For example, this is shown by the SIMS and scanning capacitance/microwave impedance microscopy (SCM/sMIM) analysis. SCM/sMIM electrically characterizes the tested device and generates maps which provide graphical representation of the dopant types and concentrations by measuring carrier movement as they are attracted to or repulsed by the probe. The SCM/sMIM maps taken from Texas Instruments Accused Products shown herein demonstrate differences in carrier concentration as a function of depth, which generate electric fields within the accused products. The contrast in the SMIM image is proportional to the capacitance of the sample under inspection, so that brighter green corresponds to higher dopant concentration, and darker green/black corresponds to lower dopant concentration. Likewise, the SCM images above show doping concentration and doping type as indicated in the legends to the right.

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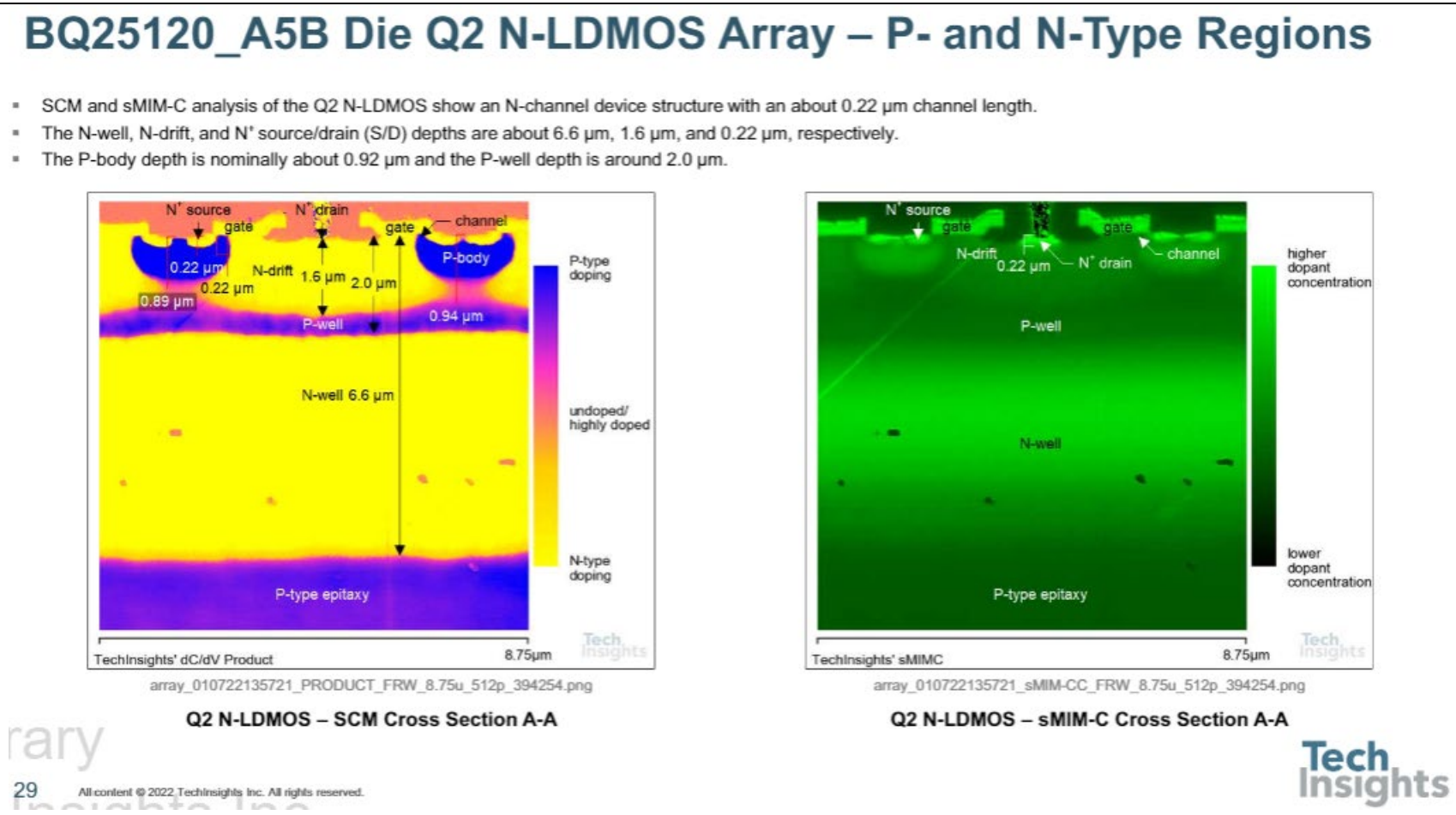
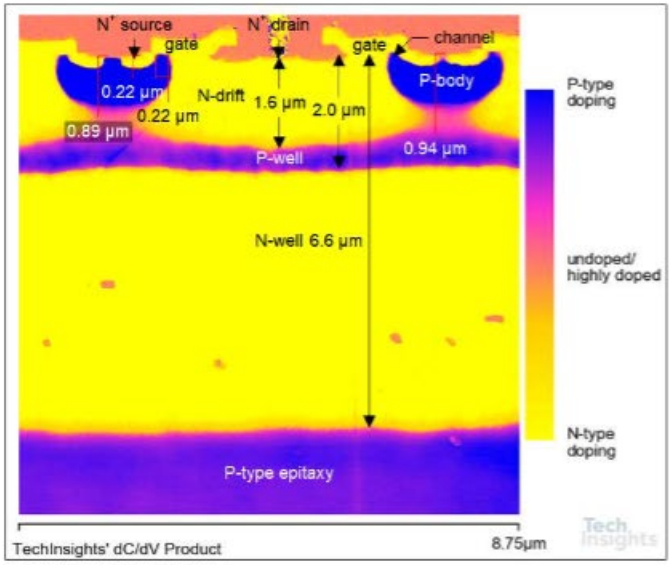
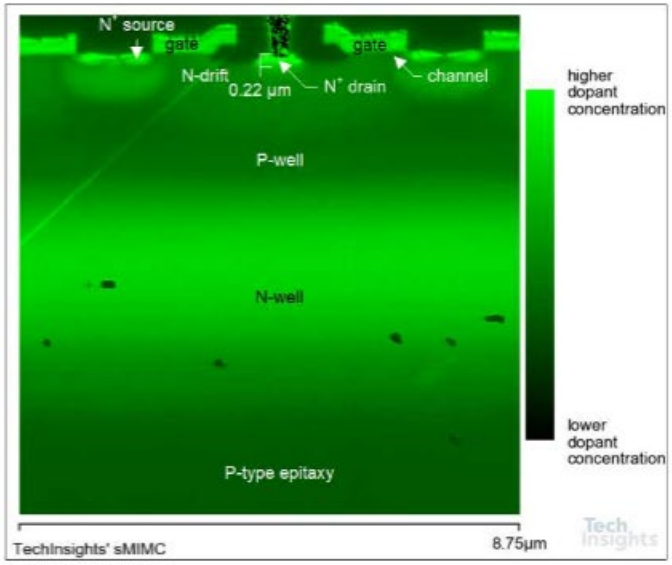
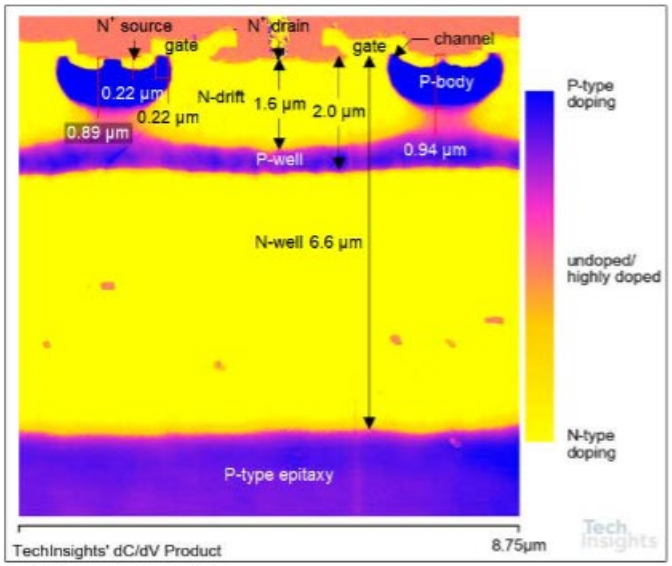
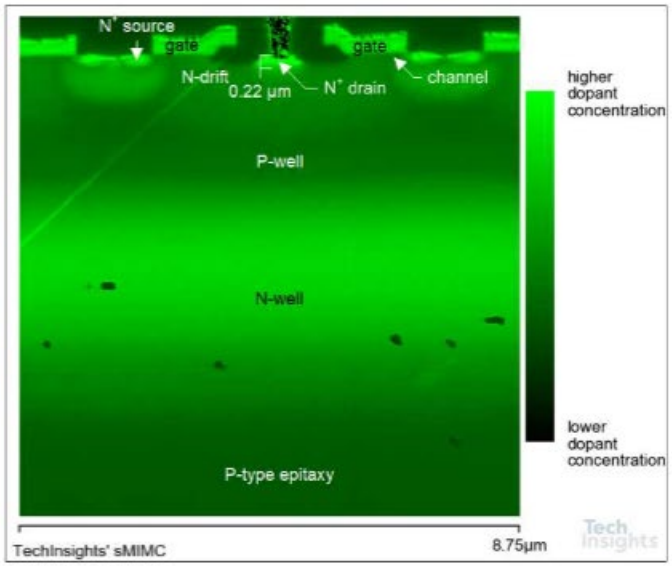
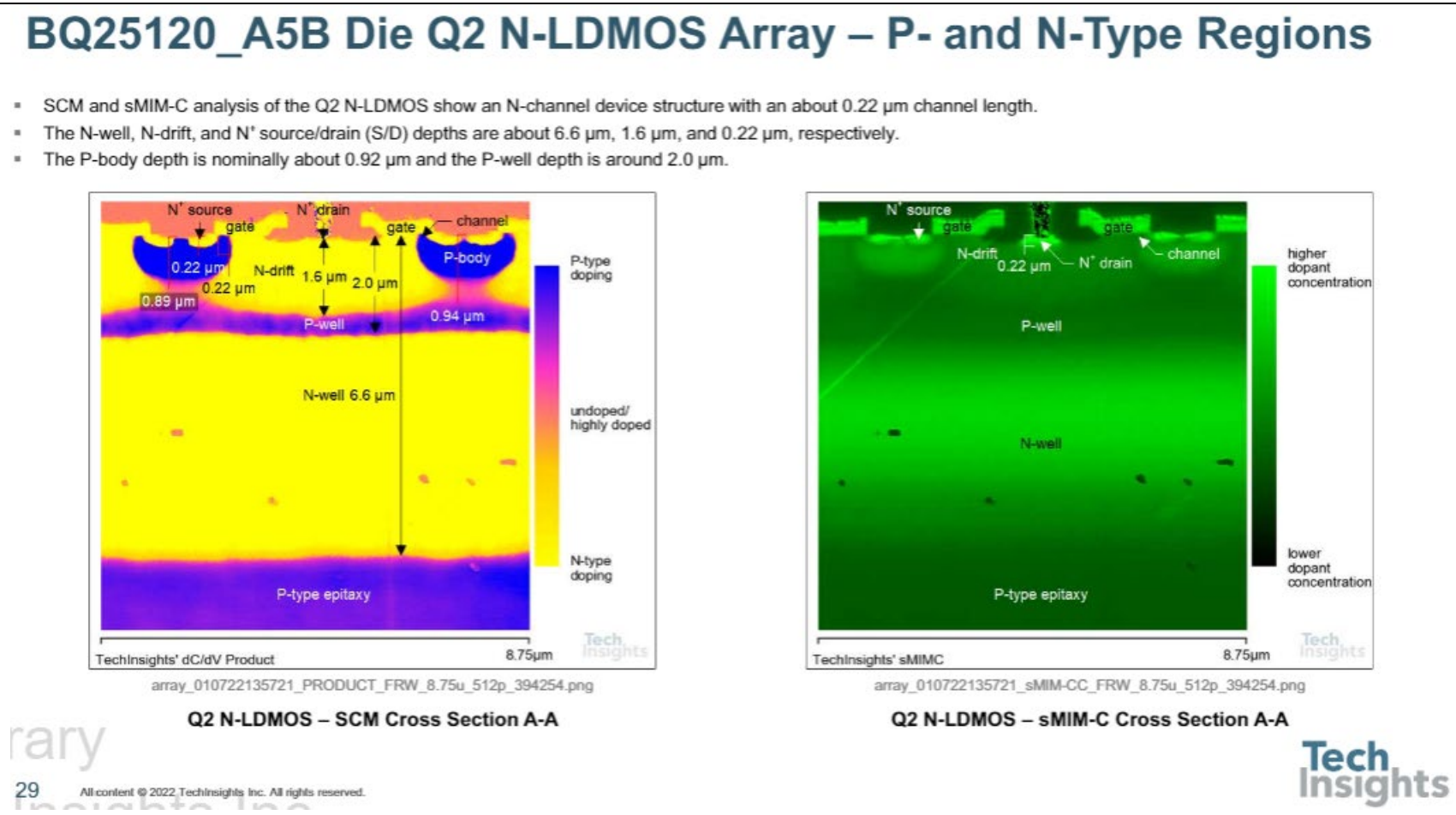
<tr>
<td></td>
<td>


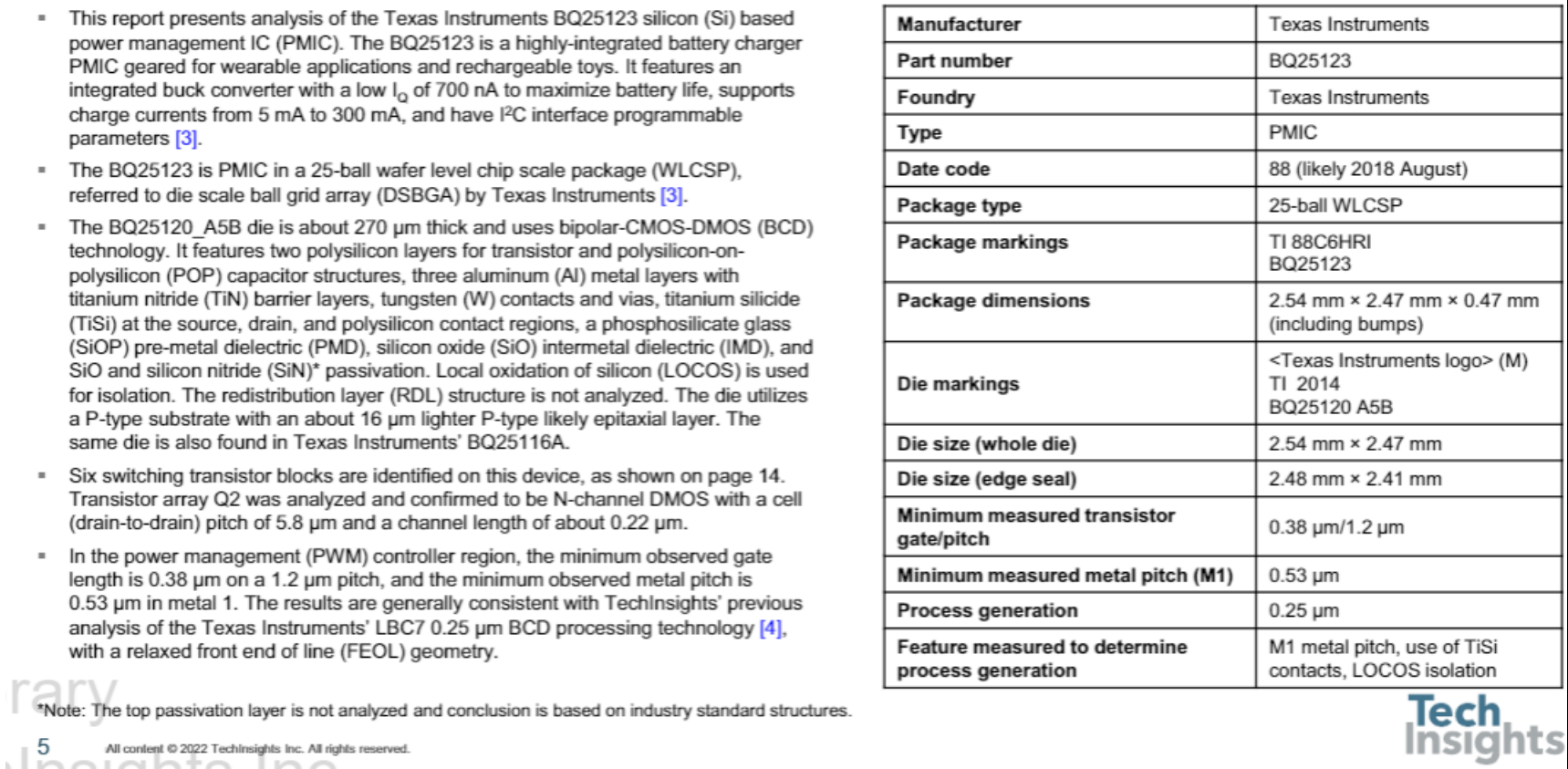
BQ25123 Report at 29.</td>
</tr>
<tr>
<td>[Claim 1, Element 6] at least one well region adjacent to the first or second active region containing at least one</td>
<td>The Texas Instruments Accused Products meet this limitation. See above at Element 1. For example, this is shown by the SIMS and scanning capacitance/microwave impedance microscopy (SCM/sMIM) analysis. SCM/sMIM electrically characterizes the tested device and generates maps which provide graphical representation of the dopant types and concentrations by measuring carrier movement as they are attracted to or repulsed by the probe. The SCM/sMIM maps taken from Texas Instruments Accused Products shown herein demonstrate differences in carrier concentration as a function of depth, which generate electric fields within the accused products. The contrast in the SMIM image is proportional to the capacitance of the sample under inspection, so that brighter green corresponds to higher dopant concentration, and darker green/black corresponds to lower dopant concentration. Likewise, the SCM images above show doping concentration and doping type as indicated in the legends to the right. The image below shows vertical dopant grading in a well</td>
</tr>
</table>

graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.	region adjacent (N-well and P-well) to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate. **BQ25120_A5B Die Q2 N-LDMOS Array – P- and N-Type Regions** ▪ SCM and sMIM-C analysis of the Q2 N-LDMOS show an N-channel device structure with an about 0.22 µm channel length. ▪ The N-well, N-drift, and N+ source/drain (S/D) depths are about 6.6 µm, 1.6 µm, and 0.22 µm, respectively. ▪ The P-body depth is nominally about 0.92 µm and the P-well depth is around 2.0 µm.  array_010722135721_PRODUCT_FRW_8.75u_512p_394254.png **Q2 N-LDMOS – SCM Cross Section A-A**  array_010722135721_sMIM-CC_FRW_8.75u_512p_394254.png **Q2 N-LDMOS – sMIM-C Cross Section A-A** 29 All content © 2022 TechInsights Inc. All rights reserved. BQ25123 Report at 29.
2. The semiconductor device of claim 1, wherein the substrate is a	Upon information and belief, the Texas Instruments Accused Products meet this limitation. The SCM cross-section image below identifies a P-type epitaxy.

p-type substrate.	**BQ25120_A5B Die Q2 N-LDMOS Array – P- and N-Type Regions** ▪ SCM and sMIM-C analysis of the Q2 N-LDMOS show an N-channel device structure with an about 0.22 µm channel length. ▪ The N-well, N-drift, and N+ source/drain (S/D) depths are about 6.6 µm, 1.6 µm, and 0.22 µm, respectively. ▪ The P-body depth is nominally about 0.92 µm and the P-well depth is around 2.0 µm.  array_010722135721_PRODUCT_FRW_8.75u_512p_394254.png **Q2 N-LDMOS – SCM Cross Section A-A**  array_010722135721_sMIM-CC_FRW_8.75u_512p_394254.png **Q2 N-LDMOS – sMIM-C Cross Section A-A** 29 All content © 2022 TechInsights Inc. All rights reserved. BQ25123 Report at 29.
3. The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a	Upon information and belief, the substrate of the Texas Instruments Accused Products has epitaxial silicon on top of a nonepitaxial substrate. The SCM cross-section image below identifies a P-type epitaxy.

nonepitaxial substrate.	 BQ25123 Report at 29.
4. The semiconductor device of claim 1, wherein the first active region and second active region contain	The Texas Instruments Accused Products meet this limitation. As shown above, both N-well and P-wells are used in this device. The first and second active regions accordingly contain p-channel or n-channel devices. *See* Tech Insights Report images reproduced at Claim 1, Element 2.

one of either p-channel and n-channel devices.	
5. The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.	The Texas Instruments Accused Products meet this limitation. As shown above, both N-well and P-wells are used in this device, and the wells include graded dopants. The first and second active regions accordingly contain p-channel or n-channel devices. *See* Tech Insights Report images reproduced at Claim 1, Element 2.
6. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	Upon information and belief, the substrate of the Texas Instruments Accused Products have isolation regions that separate the first and second active regions. As shown in the Device Summary below, "[l]ocal oxidation of silicon (LOCOS) is used for isolation."



Device Summary

- This report presents analysis of the Texas Instruments BQ25123 silicon (Si) based power management IC (PMIC). The BQ25123 is a highly-integrated battery charger PMIC geared for wearable applications and rechargeable toys. It features an integrated buck converter with a low I_Q of 700 nA to maximize battery life, supports charge currents from 5 mA to 300 mA, and have I^2C interface programmable parameters [3].
- The BQ25123 is PMIC in a 25-ball wafer level chip scale package (WLCSP), referred to die scale ball grid array (DSBGA) by Texas Instruments [3].
- The BQ25120_A5B die is about 270 µm thick and uses bipolar-CMOS-DMOS (BCD) technology. It features two polysilicon layers for transistor and polysilicon-on-polysilicon (POP) capacitor structures, three aluminum (Al) metal layers with titanium nitride (TiN) barrier layers, tungsten (W) contacts and vias, titanium silicide (TiSi) at the source, drain, and polysilicon contact regions, a phosphosilicate glass (SiOP) pre-metal dielectric (PMD), silicon oxide (SiO) intermetal dielectric (IMD), and SiO and silicon nitride (SiN)* passivation. Local oxidation of silicon (LOCOS) is used for isolation. The redistribution layer (RDL) structure is not analyzed. The die utilizes a P-type substrate with an about 16 µm lighter P-type likely epitaxial layer. The same die is also found in Texas Instruments' BQ25116A.
- Six switching transistor blocks are identified on this device, as shown on page 14. Transistor array Q2 was analyzed and confirmed to be N-channel DMOS with a cell (drain-to-drain) pitch of 5.8 µm and a channel length of about 0.22 µm.
- In the power management (PWM) controller region, the minimum observed gate length is 0.38 µm on a 1.2 µm pitch, and the minimum observed metal pitch is 0.53 µm in metal 1. The results are generally consistent with TechInsights' previous analysis of the Texas Instruments' LBC7 0.25 µm BCD processing technology [4], with a relaxed front end of line (FEOL) geometry.

Manufacturer	Texas Instruments
Part number	BQ25123
Foundry	Texas Instruments
Type	PMIC
Date code	88 (likely 2018 August)
Package type	25-ball WLCSP
Package markings	TI 88C6HRI BQ25123
Package dimensions	2.54 mm × 2.47 mm × 0.47 mm (including bumps)
Die markings	<Texas Instruments logo> (M) TI 2014 BQ25120 A5B
Die size (whole die)	2.54 mm × 2.47 mm
Die size (edge seal)	2.48 mm × 2.41 mm
Minimum measured transistor gate/pitch	0.38 µm/1.2 µm
Minimum measured metal pitch (M1)	0.53 µm
Process generation	0.25 µm
Feature measured to determine process generation	M1 metal pitch, use of TiSi contacts, LOCOS isolation

*Note: The top passivation layer is not analyzed and conclusion is based on industry standard structures.

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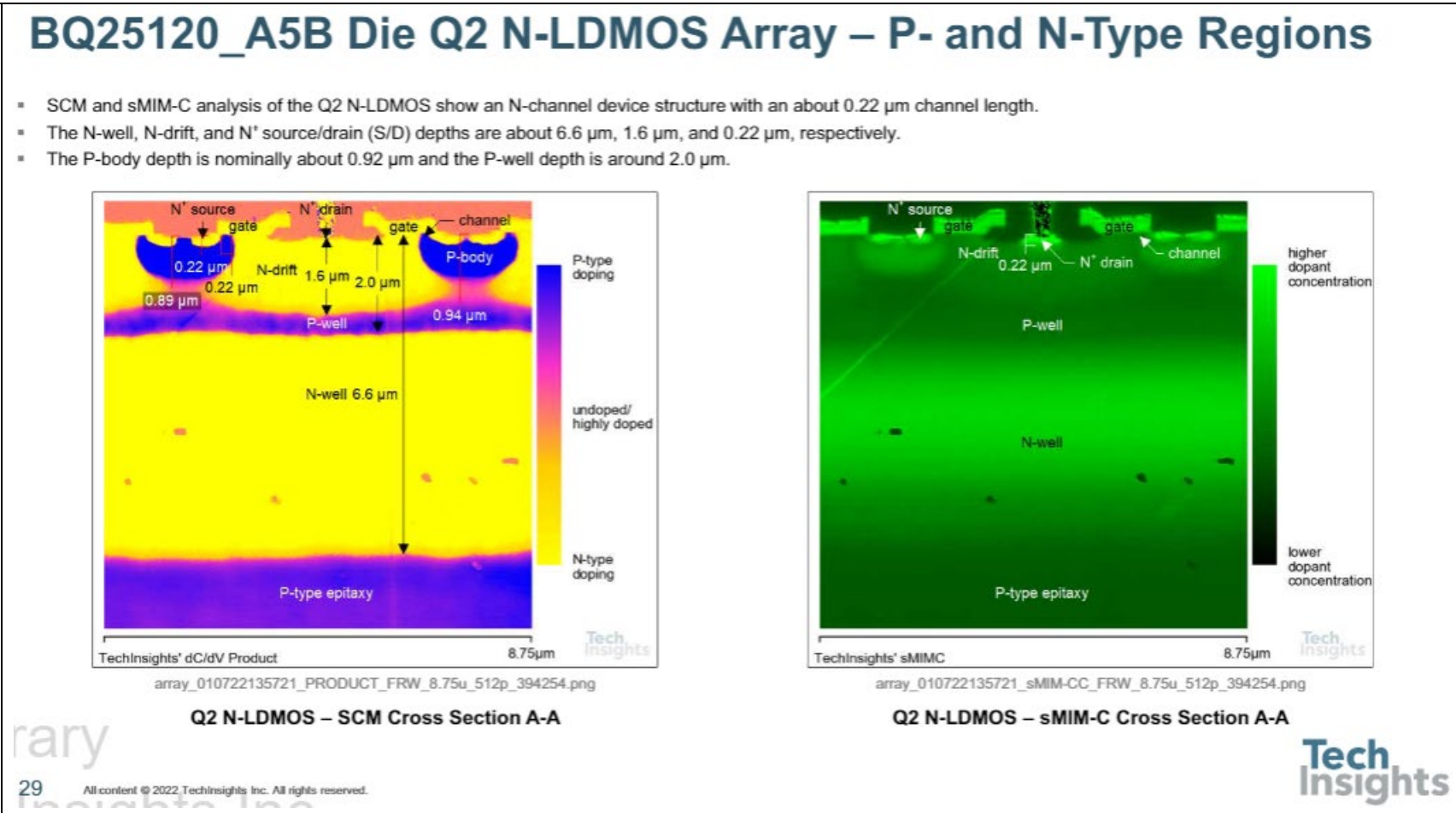
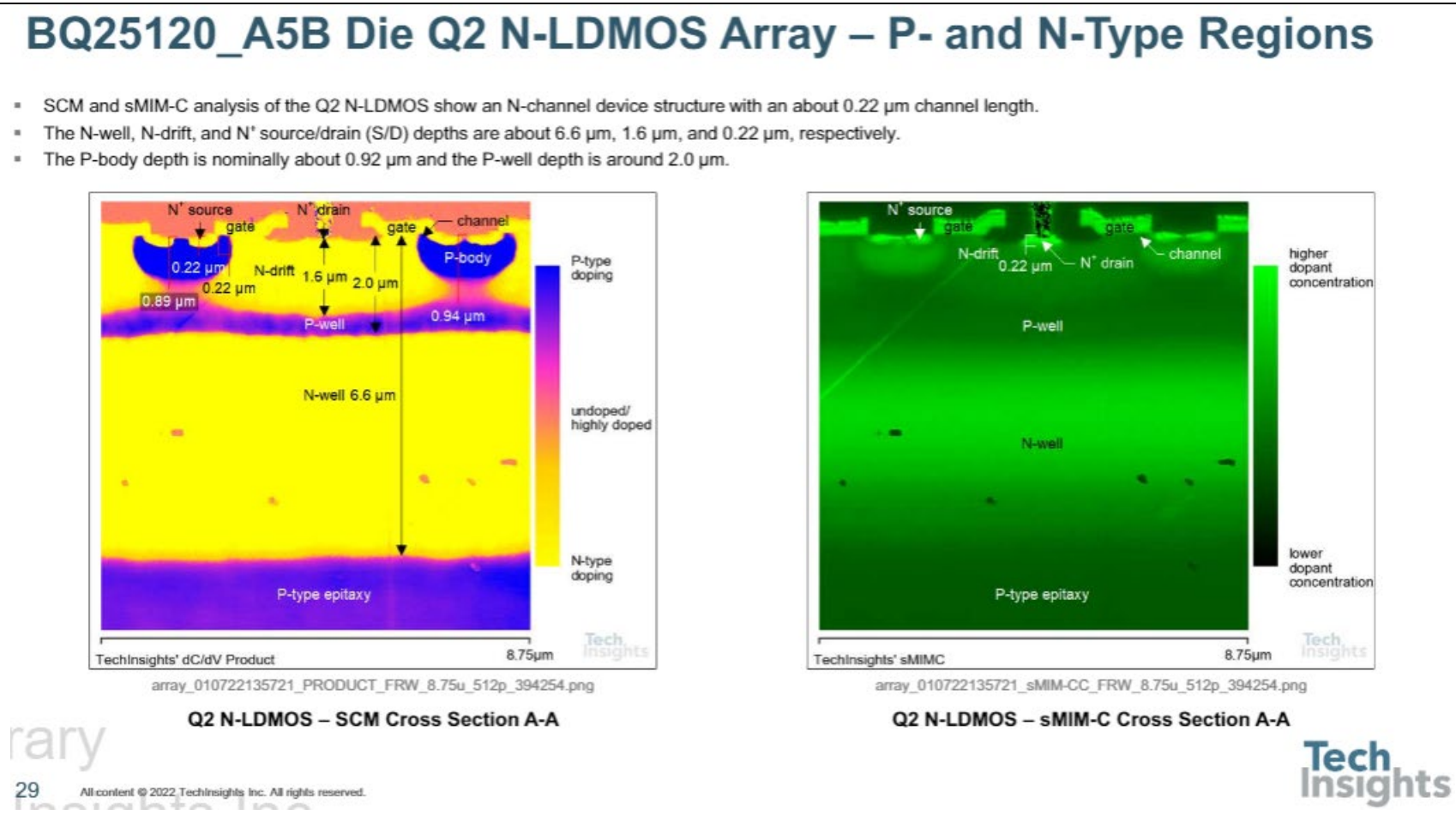
Tech Insights

BQ25123 Report at 5.

7. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion	Upon information and belief, the graded dopant is fabricated with an ion implantation process. For example, ion implantation is the prevalent process for implementing doping in semiconductor devices, and is believed to be used for the Texas Instruments Accused Products. Additionally Texas Instruments has multiple patents disclosing ion implantation used in semiconductor fabrication, including U.S. Patent No. 9,064,903 which states that "MOS transistors are generally constructed by way of a counter-doping ion implantation into the channel region...." Because Texas Instruments has patents disclosing this practice, and because it is well known in the art, Texas Instruments Accused Products likely meet this limitation. Information about the fabrication process for the Texas Instruments Accused Products, including usage of an ion implantation process, is in the possession of Defendant and is expected to be obtained through discovery.

implantation process.	
8. The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	The Texas Instruments Accused Products meet this limitation. *See* above at Claim 1, Elements 1-3.
9. The semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The Texas Instruments Accused Products meet this limitation. The SIMS image below indicates graded dopant regions in the first active region or the second active region that are both p-type and n-type.

	 BQ25123 Report at 29.
12. The semiconductor device of claim 1, wherein dopants of the graded dopant region in the well region are	The Texas Instruments Accused Products meet this limitation. The SCM image below indicates graded dopant regions in well regions that are both p-type and n-type.

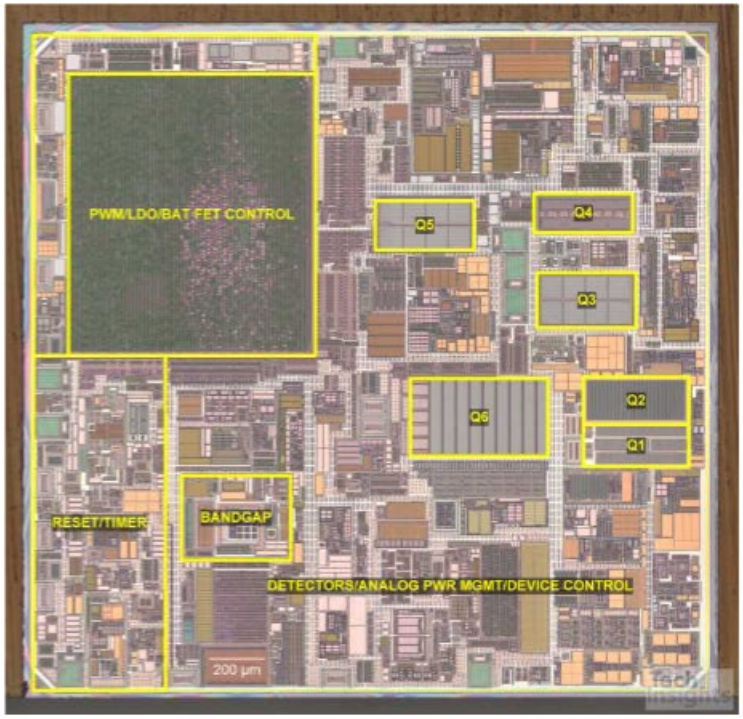
both p-type and n-type.	 BQ25123 Report at 29.
13.The semiconductor device of claim 1, wherein the transistors which can be formed in the first and	The Texas Instruments Accused Products meet this limitation. As discussed above for Claim 1, the Texas Instruments Accused Products include first and second active regions. Upon information and belief, CMOS transistors formed in the first and second active regions, the CMOS transistors requiring a source, a drain, a gate, and a channel region. Details regarding transistors used are in the possession of Defendants and are expected to be obtained through discovery.

second active regions are CMOS transistors requiring at least a source, a drain, a gate and a channel.	
15. The semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.	The Texas Instruments Accused Products meet this limitation. *See* Claims 3 (regarding nonepitaxial substrate), 13 (regarding CMOS).
17. The semiconductor device of claim 1, wherein the device is a logic device.	The Texas Instruments Accused Products meet this limitation. As shown in the block diagram of the figure below, the BQ25123 includes a power management and device control region which constitutes a logic device.

BQ25120_A5B Die Photograph at the Gate Layer

- The die was deprocessed to the polysilicon gate level.
- The die utilization is characterized in the table below.

Functional Description	Length (mm)	Width (mm)	Area (mm^2)	Percentage of Die
Q1 (switching transistor connected between the DC input supply pin [IN] and the high-side bypass connection pin [PMID])	0.15	0.39	0.06	1.0
Q2 (switching transistor connected between the DC input supply pin [IN] and the high-side bypass connection pin [PMID])	0.17	0.39	0.07	1.1
Q3 (switching transistor connected between the high-side bypass connection pin [PMID] and the inductor connection pin [SW])	0.20	0.36	0.07	1.2
Q4 (switching transistor connected between the inductor connection pin [SW] and the PGND pin [PGND])	0.14	0.36	0.05	0.9
Q5 (switching transistor connected between the input to the load switch pin [VINLS] and the load switch/LDO output pin [LDO])	0.18	0.36	0.06	1.1
Q6 (switching transistor connected between the battery connection pin [BAT] and the high-side bypass connection pin [PMID])	0.28	0.50	0.14	2.4
Bandgap bias generator	0.31	0.40	0.12	2.1
Reset/timer block	1.22	0.48	0.59	9.8
Detectors/analog PWR MGMT/device control block	Irregular		3.50	58.5
PWM control/LDO/BAT FET control	1.03	0.90	0.92	15.5
Control I/O	Irregular		0.28	4.6
Others			0.12	1.8
Total die	2.41	2.48	5.98	100.0



BQ25123YFPT_BQ25120_BPoly_blocks.png

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BQ25123 Report at 14.

~~18. The semiconductor device of claim 17, wherein the device is central processing unit.~~

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

[Claim 20, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Texas Instruments Accused Products include/comprise a semiconductor device. *See* above at Claim 1, Preamble.
[Claim 20, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The Texas Instruments Accused Products meet this limitation. *See* Claim 1, Element 1.
[Claim 20, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The Texas Instruments Accused Products meet this limitation. *See* Claim 1, Element 2. Upon information and belief, transistors can be formed in the surface of the first active region. Details regarding formation of transistors are in the possession of Defendants and are expected to be obtained through discovery.
[Claim 20, Element 3] a second active region separate from the first active region disposed	The Texas Instruments Accused Products meet this limitation. *See* Claim 1, Element 3. Upon information and belief, transistors can be formed in the surface of the first active region. Details regarding formation of transistors are in the possession of Defendants and are expected to be obtained through discovery.

adjacent to the first active region and within which transistors can be formed in the surface thereof;	
[Claim 20, Element 4] transistors formed in at least one of the first active region or second active region;	The Texas Instruments Accused Products meet this limitation. *See* Claim 1, Element 4.
[Claim 20, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate; and	The Texas Instruments Accused Products meet this limitation. *See* Claim 1, Element 5.
[Claim 20, Element 6] at least one well region adjacent to the first or second active region containing at least one	The Texas Instruments Accused Products meet this limitation. *See* above at Claim 1, Element 6.

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.	
22. The semiconductor device of claim 20, wherein the substrate is a p-type substrate.	The Texas Instruments Accused Products meet this limitation. *See* Claim 2.
23. The semiconductor device of claim 20, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The Texas Instruments Accused Products meet this limitation. *See* Claim 3.
24. The semiconductor device of claim 20, wherein the first active region and second active region contain at least one of either p-	The Texas Instruments Accused Products meet this limitation. *See* Claim 4.

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

channel and n-channel devices.	
25.The semiconductor device of claim 20, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	The Texas Instruments Accused Products meet this limitation. *See* Claim 5.
26. The semiconductor device of claim 20, wherein the first active region and second active region are each separated by at least one isolation region.	The Texas Instruments Accused Products meet this limitation. *See* Claim 6.
27. The semiconductor device of claim 20, wherein dopants of the	The Texas Instruments Accused Products meet this limitation. *See* Claim 9.

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

graded dopant concentration in the first active region or the second active region are either p-type or n-type.	
31. The semiconductor device of claim 20, wherein the graded dopant is fabricated with an ion implantation process.	The Texas Instruments Accused Products meet this limitation. *See* Claim 7.
32. The semiconductor device of claim 20, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.	The Texas Instruments Accused Products meet this limitation. *See* Claim 13.
34. The semiconductor device of claim 20, wherein the device is a logic device.	The Texas Instruments Accused Products meet this limitation. See above, Claim 17.
~~35. The semiconductor device of~~	

~~claim 34, wherein the device is central processing unit.~~	

Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
[Claim 1, Preamble] A VLSI semiconductor device, comprising:	To the extent the preamble is a limitation, the Texas Instruments Accused Products include a VLSI semiconductor device. The Texas Instruments BQ25123 Battery Charger Power Management IC ("BQ25123") discussed for claim 1 of Exhibit A-1 is a semiconductor device (*see* Exhibit A-1, Claim 1, Preamble) with transistors, and is a VLSI semiconductor device upon information and belief. Details regarding transistor count are in the possession of the Defendants and are expected to be obtained through discovery. The Texas Instruments BQ25123 is representative of the Texas Instruments Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other Texas Instruments Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '222 patent (and the other asserted patents). For example, the other Texas Instruments Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '222 patent (and the other asserted patents). The claimed invention would have application in numerous types of Texas Instruments products, including, but not limited to, amplifiers, audio processors, digital-to-analog converters, analog-to-digital converters, digital clocks, interface ICs, isolation ICS, microcontrollers and processors, digital signal processors, digital light processors, motor drivers, power management, switches & multiplexers, radio frequency and microwave ICs, wireless connectivity ICs, logic & voltage translation, sensors, and other ICs, because such products would benefit from, among other things, improved switching time for transistors in the device. Therefore, upon information and belief the other Texas Instruments Accused Products contain similar features as the Texas Instruments BQ25123 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other Texas Instruments Accused Products contain similar features as the Texas Instruments BQ25123, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having a surface;	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 1.
[Claim 1, Element 2] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 2.
[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 3.

Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region;	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 4.
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 5. *See* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 1, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-2, Claim 1, Element 6. Upon information and belief, at least some of the transistors form digital logic of the VLSI semiconductor device. For example, transistors are commonly used to implement digital logic, e.g., for controlling access to memory components/functionality. Details regarding transistors in the Texas Instruments Accused Products are in the possession of the Defendants and are expected to be obtained through discovery. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
2. The VLSI semiconductor device of claim 1, wherein the substrate is a p-type substrate.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 2.
3. The VLSI semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 4.
4. The VLSI semiconductor device of claim 1, wherein the first active region and second	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 5; Exhibit A-2, Claim 4. Upon information and belief, the first and second active regions contain digital logic as claimed. *See* above at Claim 1, Element 6.

Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
active region contain digital logic formed by one of either p-channel and n-channel devices.	
5. The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n−wells or p−wells, respectively, and each well has at least one graded dopant.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 6.
6. The VLSI semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 7.
7. The VLSI semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 8.
8. The VLSI semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Elements 1-3.
9. The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-2, Claim 9.
13. The VLSI semiconductor device of claim 1, wherein the	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-2, Claim 13. Upon information and belief, the transistors which can be formed in the first and second active regions are CMOS digital logic transistors as claimed. *See* above at Claim 1, Element 6.

Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
transistors which can be formed in the first and second active regions are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.	
15. The VLSI semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-2, Claim 15.
16. The VLSI semiconductor device of claim 1, wherein the device is a flash memory.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-2, Claim 16.
17. The VLSI semiconductor device of claim 1, wherein the device comprises digital logic and capacitors.	The Texas Instruments Accused Products meet this limitation. Upon information and belief, the semiconductor device comprises digital logic and capacitors. *See* above at Claim 1, Element 6 (discussion regarding digital logic). Details regarding digital logic and capacitors in the Texas Instruments Accused Products are in the possession of the Defendants and are expected to be obtained through discovery.
20. The VLSI semiconductor device of claim 1, wherein each of the first and second active regions are in the lateral or vertical direction.	The Texas Instruments Accused Products meet this limitation. As shown by SEM imaging (*see* Exhibit A-1, Claim 1, Elements 1-3), each of the first and second active regions are in the lateral or vertical direction.
[Claim 21, Preamble] A VLSI semiconductor device, comprising:	To the extent the preamble is a limitation, the Texas Instruments Accused Products include a semiconductor device. *See* above at Claim 1, Preamble.
[Claim 21, Element 1] a substrate of a first doping type at a first doping level having a surface;	The Texas Instruments Accused Products meet this limitation. *See* above at Claim 1, Element 1.
[Claim 21, Element 2] a first active region disposed adjacent the surface of the substrate with a second doping type opposite in	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 9, Element 2.

Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
conductivity to the first doping type and within which transistors can be formed in the surface thereof;	
[Claim 21, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 9, Element 3.
[Claim 21, Element 4] transistors formed in at least one of the first active region or second active region;	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 4.
[Claim 21, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and	The Texas Instruments Accused Products meet this limitation. *See* above at Claim 1, Element 5. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 21, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-2, Claim 1, Element 6. As shown by SCM/sMIM analysis (*see* Exhibit A-1, Claim 1, Element 1), the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof. For example, the quasilinear nature of the concentration is shown in the SCM/sMIM graph discussed at Exhibit A-1, Claim 1, Element 5. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
23. The VLSI semiconductor device of claim 21, wherein the substrate is a p-type substrate.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 2.
24. The VLSI semiconductor device of claim 21, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 4.
25. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 5.
26. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain either p-channel or n-channel devices in n−wells or p−wells, respectively, and each well has at least one graded dopant.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 6.
27. The VLSI semiconductor device of claim 21, wherein the first active region and second active region are each separated by at least one isolation region.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 7.
28. The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-2, Claim 9.
32. The VLSI semiconductor device of claim 21, wherein the	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 8.

Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
graded dopant is fabricated with an ion implantation process.	
33. The VLSI semiconductor device of claim 21, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-2, Claim 15.
34. The VLSI semiconductor device of claim 21, wherein the device is a flash memory.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-2, Claim 16.
38. The VLSI semiconductor device of claim 21, wherein each of the first and second active regions are in the lateral or vertical direction.	The Texas Instruments Accused Products meet this limitation. See above at Claim 20.
[Claim 39, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Texas Instruments Accused Products include a semiconductor device. *See* Exhibit A-1, Claim 1, Preamble.
[Claim 39, Element 1] a substrate of a first doping type at a first doping level;	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 1.
[Claim 39, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 2.
[Claim 39, Element 3] a second active region separate from the first active region disposed adjacent to the first active region	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 3.

Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
and within which transistors can be formed;	
[Claim 39, Element 4] transistors formed in at least one of the first active region or second active region; and	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 4.
[Claim 39, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 5; *see* above at Claim 21, Element 5. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
40. The semiconductor device of claim 39 further comprising at least one well region adjacent to the first or second active region and containing at least one graded dopant region, the graded dopant region to aid carrier movement from any region in the well to the substrate area where there is no well.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-2, Claim 1, Element 6. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 41, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Texas Instruments Accused Products include a semiconductor device. *See* above at Claim 39, Preamble.
[Claim 41, Element 1] a substrate of a first doping type at a first doping level;	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 1.
[Claim 41, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in	The Texas Instruments Accused Products meet this limitation. *See* above at Claim 39, Element 2.

Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
conductivity to the first doping type and within which transistors can be formed;	
[Claim 41, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Texas Instruments Accused Products meet this limitation. *See* above at Claim 39, Element 3.
[Claim 41, Element 4] transistors formed in at least one of the first active region or second active region; and	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 4.
[Claim 41, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant acceptor concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	The Texas Instruments Accused Products meet this limitation. *See* above at Claim 1, Element 5. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 42, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Texas Instruments Accused Products include a semiconductor device. *See* above at Claim 39, Preamble.
[Claim 42, Element 1] a substrate of a first doping type at a first doping level;	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 1.
[Claim 42, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Texas Instruments Accused Products meet this limitation. *See* above at Claim 39, Element 2.

Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
[Claim 42, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Texas Instruments Accused Products meet this limitation. *See* above at Claim 39, Element 3.
[Claim 42, Element 4] transistors formed in at least one of the first active region or second active region; and	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 4.
[Claim 42, Element 5] at least a portion of at least one of the first and second active regions having at least one graded donor dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	The Texas Instruments Accused Products meet this limitation. SCM/sMIM analysis (*see* Exhibit A-1, Claim 1, Element 5) reveals at least one graded dopant acceptor concentration (e.g., concentration in n-well) as claimed. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 44, Preamble] A CMOS Semiconductor device comprising:	To the extent the preamble is a limitation, the Texas Instruments Accused Products include a CMOS Semiconductor device. *See* Exhibit A-1, Claim 1, Preamble; Exhibit A-1, Claim 18.
[Claim 44, Element 1]: a surface layer;	The Texas Instruments Accused Products meet this limitation. *See* above at Claim 21, Element 1.
[Claim 44, Element 2] a substrate;	The Texas Instruments Accused Products meet this limitation. *See* above at Claim 44, Element 1.
[Claim 44, Element 3] an active region including a source and a drain, disposed on one surface of the surface layer;	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Element 2 (discussion of active region); Exhibit A-1, Claim 18 (discussion of source and drain).

Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
[Claim 44, Element 4] a single drift layer disposed between the other surface of the surface layer and the substrate, the drift layer having a graded concentration of dopants extending between the surface layer and the substrate, the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions; and	The Texas Instruments Accused Products meet this limitation. *See* above at Claim 21, Element 5. Upon information and belief, the drift layer has a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions as claimed, as a result of the above-discussed graded concentration of dopants. Details regarding electric field characteristics are in the possession of the Defendants and are expected to be obtained through discovery. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 44, Element 5] at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions.	The Texas Instruments Accused Products meet this limitation. *See* above at Claim 21, Element 6. The well region (discussed above for Claim 21, Element 6) has a graded concentration of dopants. Upon information and belief, the well region is disposed in the single drift layer, and it has a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions as claimed, as a result of the well region's graded concentration of dopants. Details regarding electric field characteristics are in the possession of the Defendants and are expected to be obtained through discovery. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

Exhibit A-4 to Greenthread's Complaint

U.S. Patent No. 8,421,195	Accused Products
[Claim 1, Preamble] A CMOS Semiconductor device comprising:	To the extent the preamble is a limitation, the Texas Instruments Accused Products include a CMOS semiconductor device. The Texas Instruments BQ25123 Battery Charger Power Management IC ("BQ25123") discussed for claim 1 of Exhibit A-3 is a semiconductor device (*see* Exhibit A-1, Claim 1, Preamble and Exhibit A-3, Claim 44, Preamble) with transistors, and is a CMOS semiconductor device upon information and belief. The Texas Instruments BQ25123 is representative of the Texas Instruments Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other Texas Instruments Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '195 patent (and the other asserted patents). For example, the other Texas Instruments Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '195 patent (and the other asserted patents). The claimed invention would have application in numerous types of Texas Instruments products, including, but not limited to, amplifiers, audio processors, digital-to-analog converters, analog-to-digital converters, digital clocks, interface ICs, isolation ICS, microcontrollers and processors, digital signal processors, digital light processors, motor drivers, power management, switches & multiplexers, radio frequency and microwave ICs, wireless connectivity ICs, logic & voltage translation, sensors, and other ICs, because such products would benefit from, among other things, improved switching time for transistors in the device. Therefore, upon information and belief the other Texas Instruments Accused Products contain similar features as the Texas Instruments BQ25123 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other Texas Instruments Accused Products contain similar features as the Texas Instruments BQ25123, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1] a surface layer;	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-3, Claim 44, Element 1.
[Claim 1, Element 2] a substrate;	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-3, Claim 44, Element 2.
[Claim 1, Element 3] an active region including a source and a drain, disposed on one surface of said surface layer;	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-3, Claim 44, Element 3.
[Claim 1, Element 4] a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-3, Claim 44, Element 4. Upon information and belief, the drift layer (*see* Exhibit A-3, Claim 44, Element 4) has a first static unidirectional electric drift field to aid the movement of minority carriers from the surface layer to the substrate, as claimed. Details regarding electric field characteristics are in the possession of the Defendants and are expected to be obtained through discovery. *See also* SCM/sMIM analysis reproduced at Exhibit A-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SPM/SMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

Exhibit A-4 to Greenthread's Complaint

U.S. Patent No. 8,421,195	Accused Products
unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and	
[Claim 1, Element 5] at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-3, Claim 44, Element 5. Upon information and belief, the well region has a second static unidirectional electric drift field to aid the movement of minority carriers from the surface layer to the substrate, as claimed. Details regarding electric field characteristics are in the possession of the Defendants and are expected to be obtained through discovery. *See also* SPM/SMIM analysis reproduced at Exhibit A-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SPM/SMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
2. The CMOS Semiconductor device of claim 1, wherein the said drift layer is a deeply-implanted layer.	The Texas Instruments Accused Products meet this limitation. Upon information and belief, the drift layer is a deeply-implanted layer.
3. The CMOS Semiconductor device of claim 1, wherein said drift layer is an epitaxial layer.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 4; Exhibit A-3, Claim 44, Element 4. Upon information and belief, the drift layer is grown above the substrate and is an epitaxial layer.
5. The CMOS Semiconductor device of claim 1, wherein said graded concentration follows a quasi-linear gradient.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Elements 1, 5.
6. The CMOS Semiconductor device of claim 1, wherein said graded concentration follows an exponential gradient.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Elements 1, 5.

Exhibit A-5 to Greenthread's Complaint

U.S. Patent No. 9,190,502	Accused Products
[Claim 7, Preamble] A semiconductor device comprising:	To the extent the preamble is a limitation, the Texas Instruments Accused Products include a semiconductor device. The Texas Instruments BQ25123 Battery Charger Power Management IC ("BQ25123") discussed for claim 1 of Exhibit A-1 is a semiconductor device (*see* Exhibit A-1, Claim 1, Preamble) with transistors, and is a semiconductor device upon information and belief. Details regarding transistor count are in the possession of the Defendants and are expected to be obtained through discovery. The Texas Instruments BQ25123 is representative of the Texas Instruments Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other Texas Instruments Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '502 patent (and the other asserted patents). For example, the other Texas Instruments Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '502 patent (and the other asserted patents). The claimed invention would have application in numerous types of Texas Instruments products, including, but not limited to, amplifiers, audio processors, digital-to-analog converters, analog-to-digital converters, digital clocks, interface ICs, isolation ICS, microcontrollers and processors, digital signal processors, digital light processors, motor drivers, power management, switches & multiplexers, radio frequency and microwave ICs, wireless connectivity ICs, logic & voltage translation, sensors, and other ICs, because such products would benefit from, among other things, improved switching time for transistors in the device. Therefore, upon information and belief the other Texas Instruments Accused Products contain similar features as the Texas Instruments BQ25123 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other Texas Instruments Accused Products contain similar features as the Texas Instruments BQ25123, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 7, Element 1] a surface layer;	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-4, Claim 1, Element 1.
[Claim 7, Element 2] a substrate;	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-4, Claim 1, Element 2.
[Claim 7, Element 3] an active region including a source and a drain, disposed on one surface of said surface layer;	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-4, Claim 1, Element 3.
[Claim 7, Element 4] a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants generating a first static unidirectional electric drift field to	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-4, Claim 1, Element 4. The graded concentration of dopants observed via SCM/sMIM analysis (*see* Exhibit A-1, Claim 1, Elements 1, 5) generates a first static unidirectional electric drift field to aid the movement of minority carriers, as claimed. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

Exhibit A-5 to Greenthread's Complaint

U.S. Patent No. 9,190,502	Accused Products
aid the movement of minority carriers from said surface layer to said substrate;	
[Claim 7, Element 5] and at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants generating a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-4, Claim 1, Element 5. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
8. The semiconductor device of claim 7 wherein said first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions.	The Texas Instruments Accused Products meet this limitation. Upon information and belief, the first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions. Details regarding the electric fields and active regions are in the possession of the Defendants and are expected to be obtained through discovery. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

Exhibit A-6 to Greenthread's Complaint

U.S. Patent No. 11,316,014	Accused Products
[Claim 1, Preamble] An electronic system, the system comprising:	To the extent the preamble is a limitation, the Texas Instruments Accused Products include an electronic system. *See* Exhibit A-1, Claim 1, Preamble; Exhibit A-4, Claim 1, Preamble. Each Texas Instruments Accused Product is an electronic system, because a computer is an electronic system. The Texas Instruments BQ25123 is representative of the Texas Instruments Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other Texas Instruments Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '014 patent (and the other asserted patents). For example, the other Texas Instruments Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '014 patent (and the other asserted patents). The claimed invention would have application in numerous types of Texas Instruments products, including, but not limited to, amplifiers, audio processors, digital-to-analog converters, analog-to-digital converters, digital clocks, interface ICs, isolation ICS, microcontrollers and processors, digital signal processors, digital light processors, motor drivers, power management, switches & multiplexers, radio frequency and microwave ICs, wireless connectivity ICs, logic & voltage translation, sensors, and other ICs, because such products would benefit from, among other things, improved switching time for transistors in the device. Therefore, upon information and belief the other Texas Instruments Accused Products contain similar features as the Texas Instruments BQ25123 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other Texas Instruments Accused Products contain similar features as the Texas Instruments BQ25123, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1a] at least one semiconductor device, the at least one semiconductor device including:	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-1, Claim 1, Preamble.
[Claim 1, Element 1b] a substrate of a first doping type at a first doping level having a surface;	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-3, Claim 1, Element 1.
[Claim 1, Element 1c] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-3, Claim 1, Element 2; Exhibit A-1, Claim 9, Element 2.
[Claim 1, Element 1d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-3, Claim 1, Element 3; Exhibit A-1, Claim 9, Element 3.
[Claim 1, Element 1e] transistors formed in at least one of the first	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-3, Claim 1, Element 4.

Exhibit A-6 to Greenthread's Complaint

U.S. Patent No. 11,316,014	Accused Products
active region or second active region;	
[Claim 1, Element 1f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-3, Claim 1, Element 5. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 1, Element 1g] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the semiconductor device.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-3, Claim 1, Element 6; Exhibit A-3, Claim 21, Element *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.6.
2. The system of Claim 1, wherein the substrate of the at least one semiconductor device is a p-type substrate.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-3, Claim 2.
3. The system of Claim 1, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-3, Claim 3.
4. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device contain digital logic formed by one of either p-channel and n-channel devices.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-3, Claim 4.
5. The system of Claim 1, wherein the first active region and second	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-3, Claim 5.

Exhibit A-6 to Greenthread's Complaint

U.S. Patent No. 11,316,014	Accused Products
active region of the at least one semiconductor device contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	
6. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-3, Claim 6.
7. The system of Claim 1, wherein the graded dopant is fabricated with an ion implantation process.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-3, Claim 7.
8. The system of Claim 1, wherein the first and second active regions of the at least one semiconductor device are formed adjacent the first surface of the substrate of the at least one semiconductor device.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-3, Claim 8.
9. The system of Claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-3, Claim 9.
13. The system of claim 1, wherein the transistors which can be formed in the first and second active regions of the at least one semiconductor device are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-3, Claim 13.
15. The system of Claim 1, wherein the at least one semiconductor device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-3, Claim 15.

Exhibit A-6 to Greenthread's Complaint

U.S. Patent No. 11,316,014	Accused Products
16. The system of Claim 1, wherein the at least one semiconductor device is a flash memory.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-3, Claim 16.
17. The system of Claim 1, wherein the at least one semiconductor device comprises digital logic and capacitors.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-3, Claim 17.
20. The system of Claim 1, wherein each of the first and second active regions of the at least one semiconductor device are in the lateral or vertical direction.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-3, Claim 20.
[Claim 21, Preamble] An electronic system, the system comprising:	To the extent the preamble is a limitation, the Texas Instruments Accused Products include an electronic system. *See* above at Claim 1, Preamble.
[Claim 21, Element 1a] at least one semiconductor device, the at least one semiconductor device including:	The Texas Instruments Accused Products meet this limitation. *See* above at Claim 1, Element 1a.
[Claim 21, Element 1b] a substrate of a first doping type at a first doping level having a surface;	The Texas Instruments Accused Products meet this limitation. *See* above at Claim 1, Element 1b.
[Claim 21, Element 1c] a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The Texas Instruments Accused Products meet this limitation. *See* above at Claim 1, Element 1c; Exhibit A-1, Claim 9, Element 2.
[Claim 21, Element 1d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The Texas Instruments Accused Products meet this limitation. *See* above at Claim 1, Element 1d; Exhibit A-1, Claim 9, Element 3.
[Claim 21, Element 1e] transistors formed in at least one of the first active region or second active region;	The Texas Instruments Accused Products meet this limitation. *See* above at Claim 1, Element 1e.

Exhibit A-6 to Greenthread's Complaint

U.S. Patent No. 11,316,014	Accused Products
[Claim 21, Element 1f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and	The Texas Instruments Accused Products meet this limitation. *See* above at Claim 1, Element 1f; Exhibit A-1, Claim 9, Element 5. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 21, Element 1g] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier thereof movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.	The Texas Instruments Accused Products meet this limitation. *See* above at Claim 1, Element 1g; Exhibit A-3, Claim 21, Element 6. *See also* SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
23. The system of Claim 21, wherein the substrate of the at least one semiconductor device is a p-type substrate.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-3, Claim 23.
24. The system of Claim 21, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-3, Claim 24.
25. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device contain at least one of either p-channel and n-channel devices.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-3, Claim 25.
26. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-3, Claim 26.

Exhibit A-6 to Greenthread's Complaint

U.S. Patent No. 11,316,014	Accused Products
devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	
27. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-3, Claim 27.
28. The system of Claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.	The Texas Instruments Accused Products meet this limitation. *See* Exhibit A-3, Claim 28.